

FIG. 1

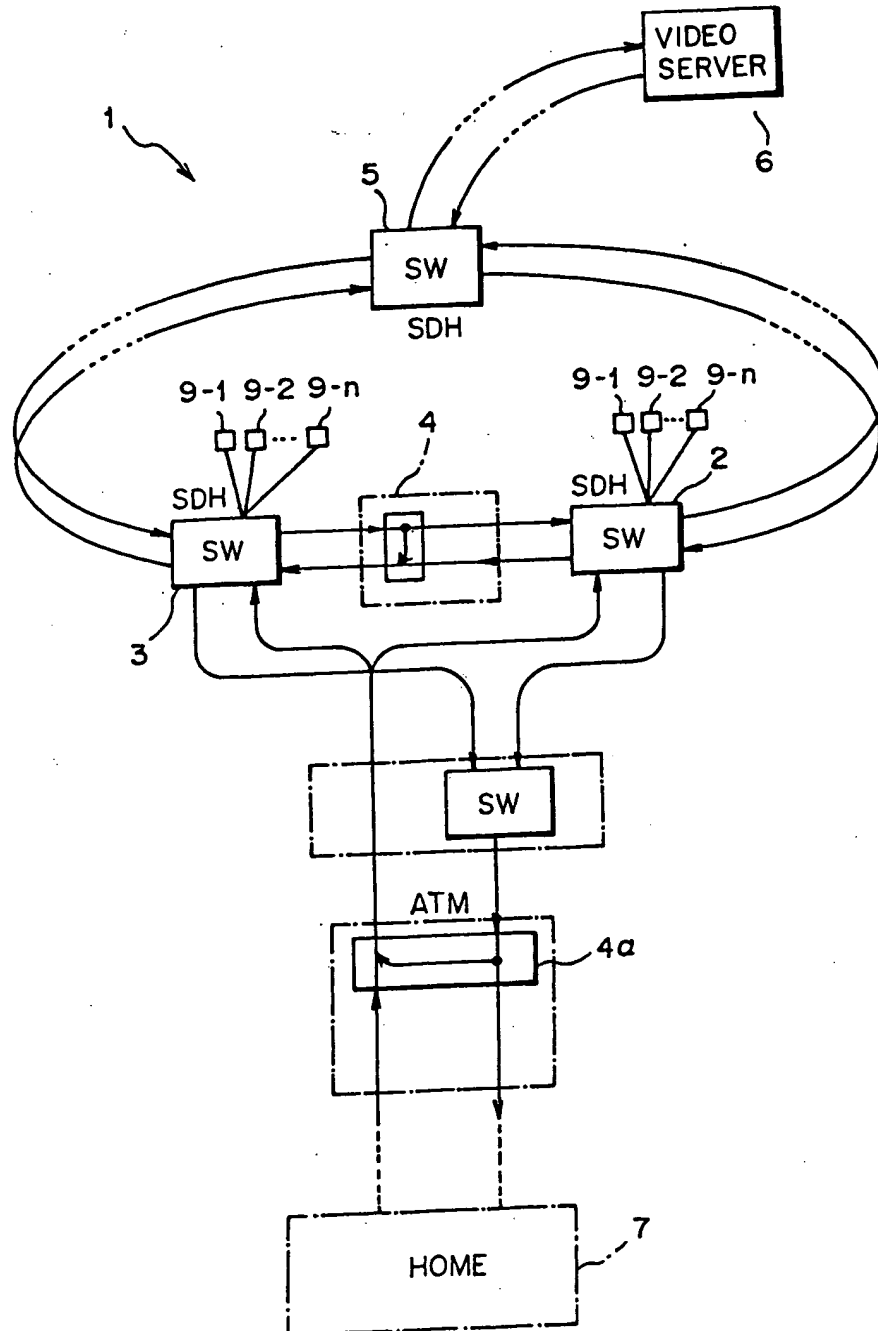


FIG. 2

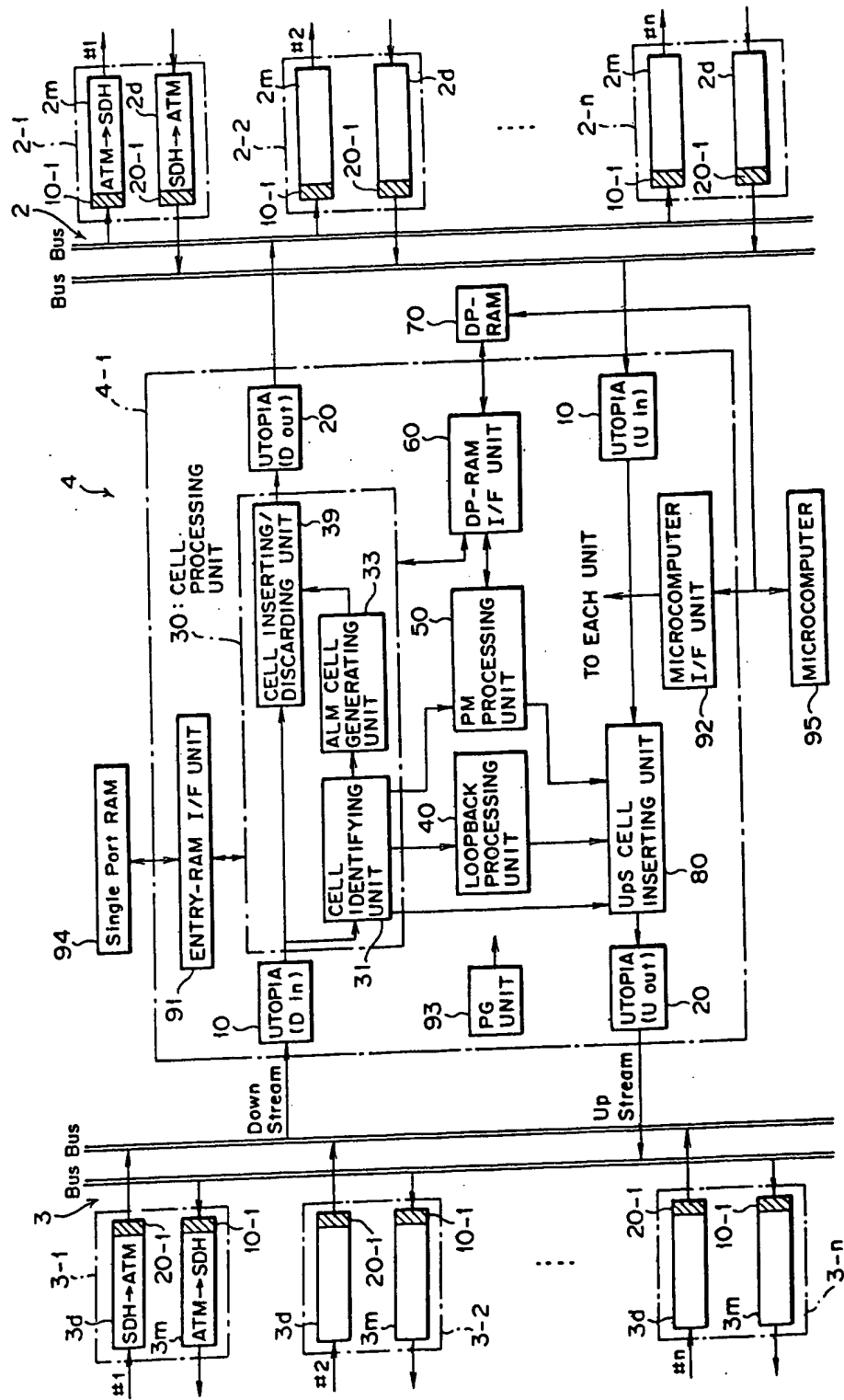


FIG. 3(a)

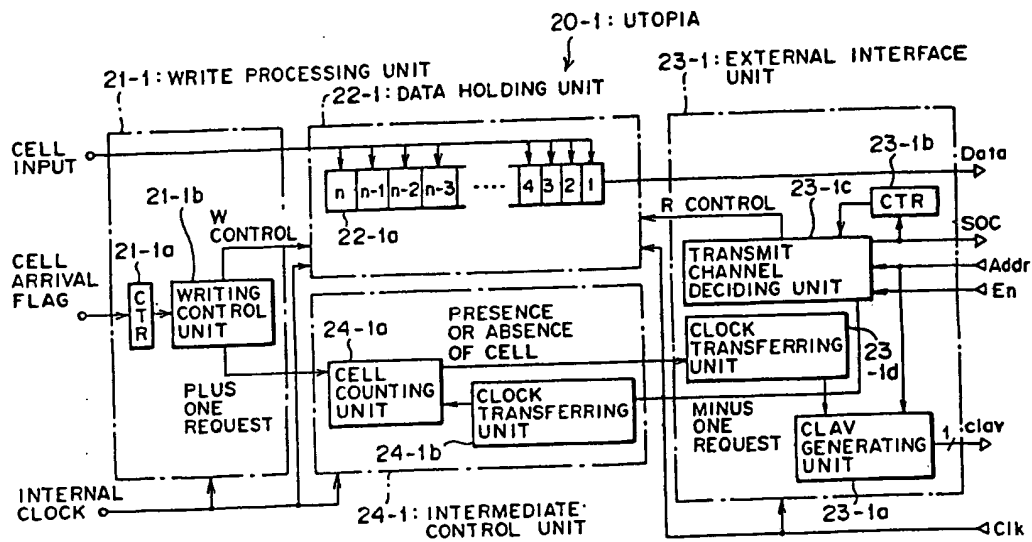


FIG. 3(b)

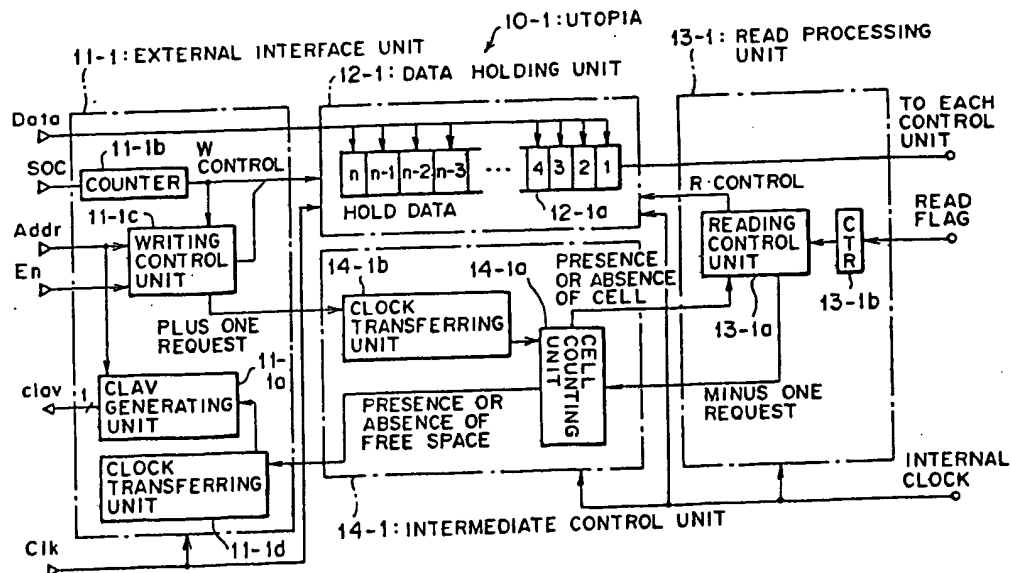


FIG. 4(a)

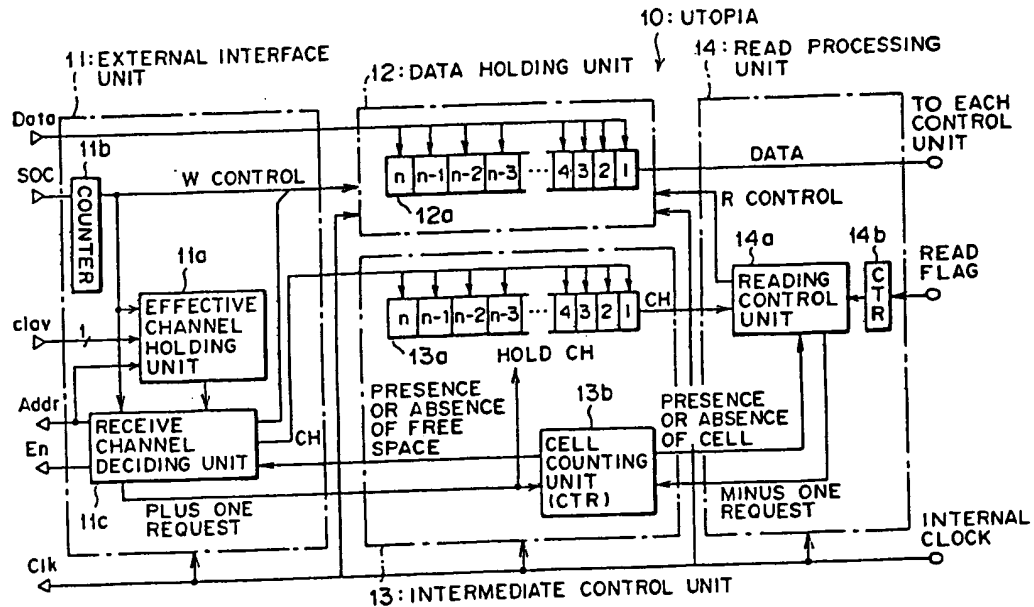


FIG. 4(b)

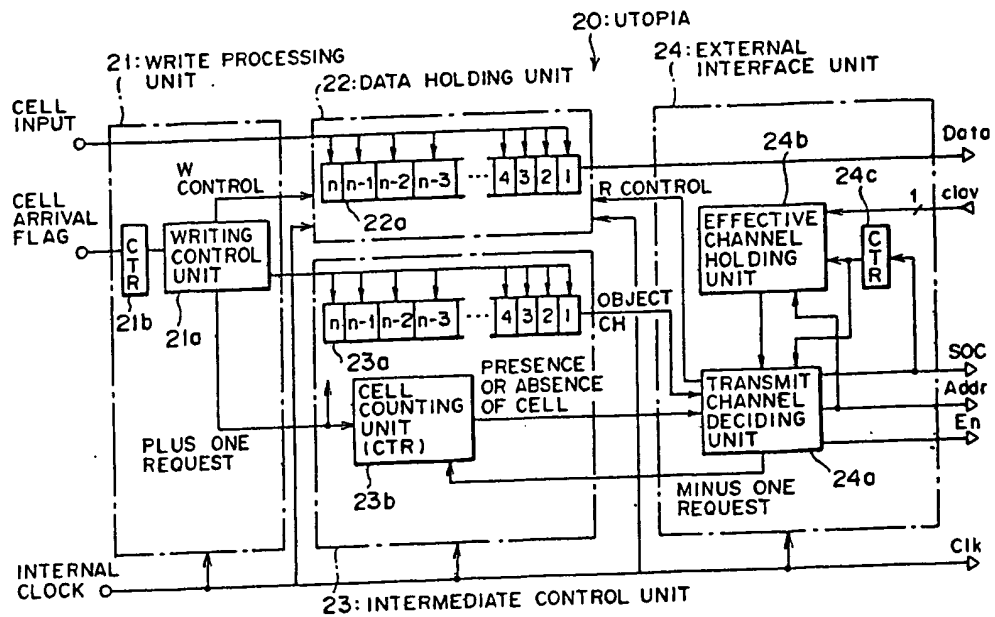


FIG. 5(a)
INPUT ON THE
DOWNSTREAM SIDE
(ASYNCHRONOUS)



FIG. 5(b)
INPUT ON THE
UPSTREAM SIDE
(ASYNCHRONOUS)

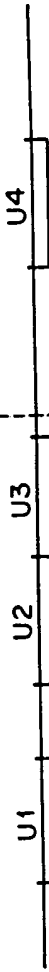


FIG. 5(c)
ATM CELL PROCESSING
UNIT REFERENCE TIMING



FIG. 5(d)
DOWNSTREAM CELL FLOW
(WITHIN ATM CELL
PROCESSING UNIT)

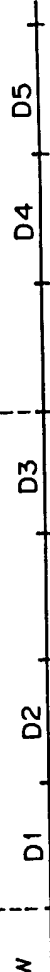
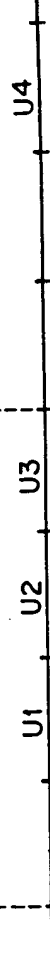


FIG. 5(e)
UPSTREAM CELL FLOW
(WITHIN ATM CELL
PROCESSING UNIT)



LEADING CELL

FIG.6

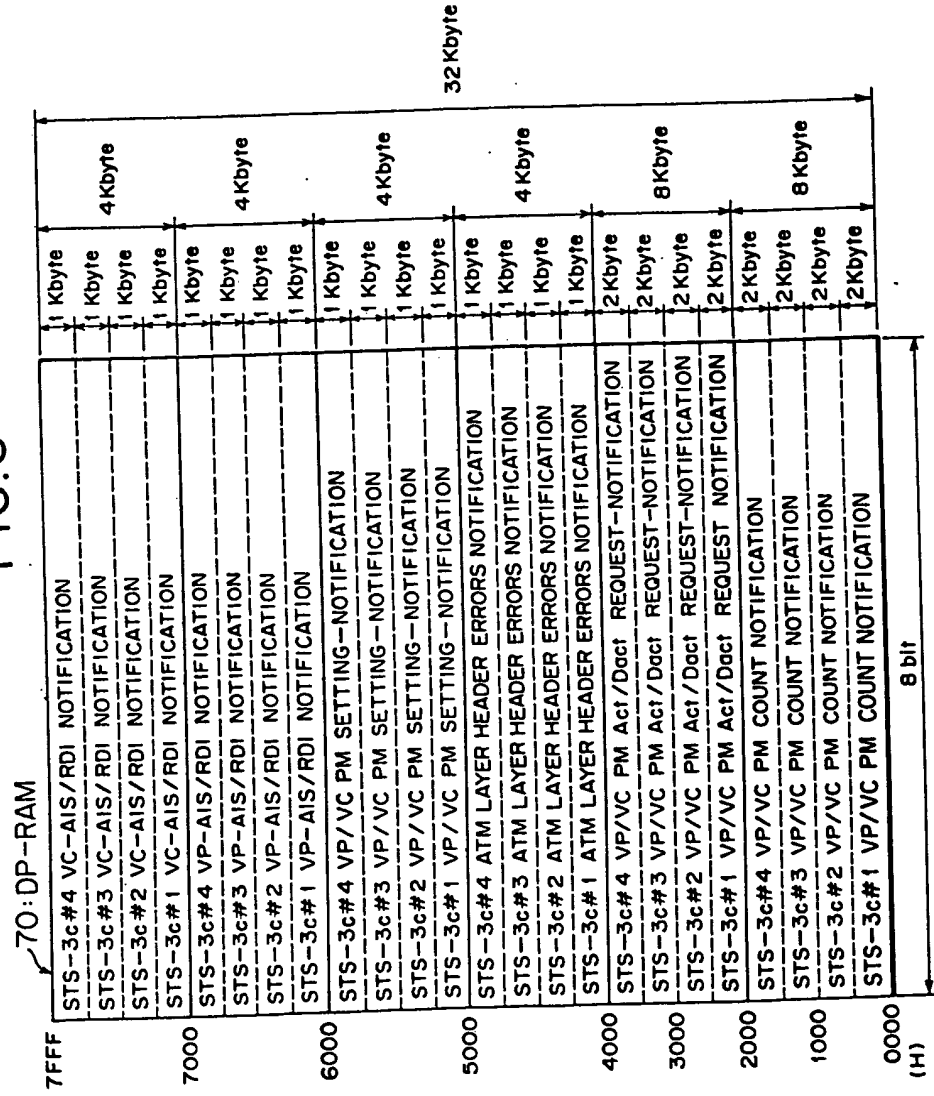


FIG. 7

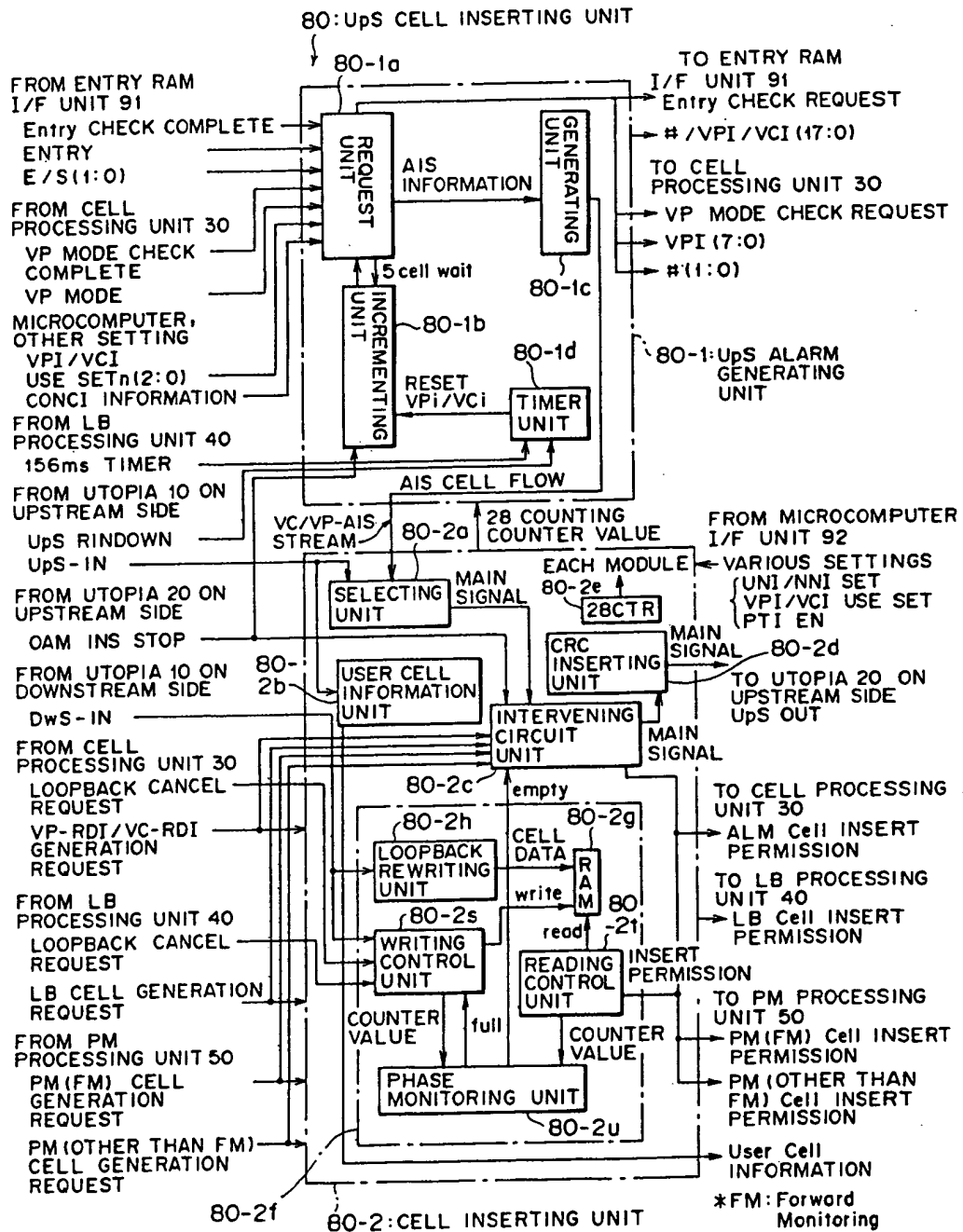


FIG. 8

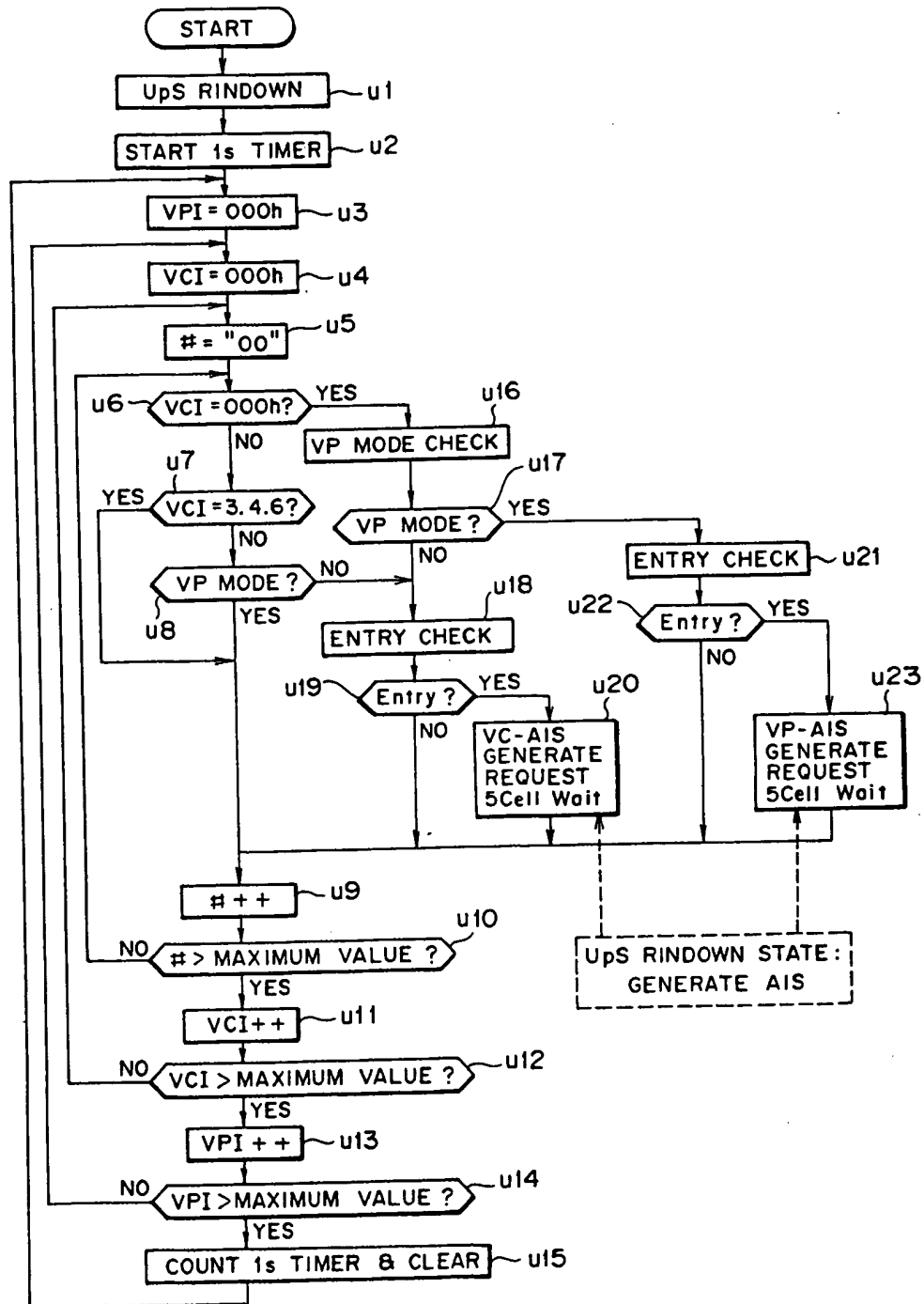
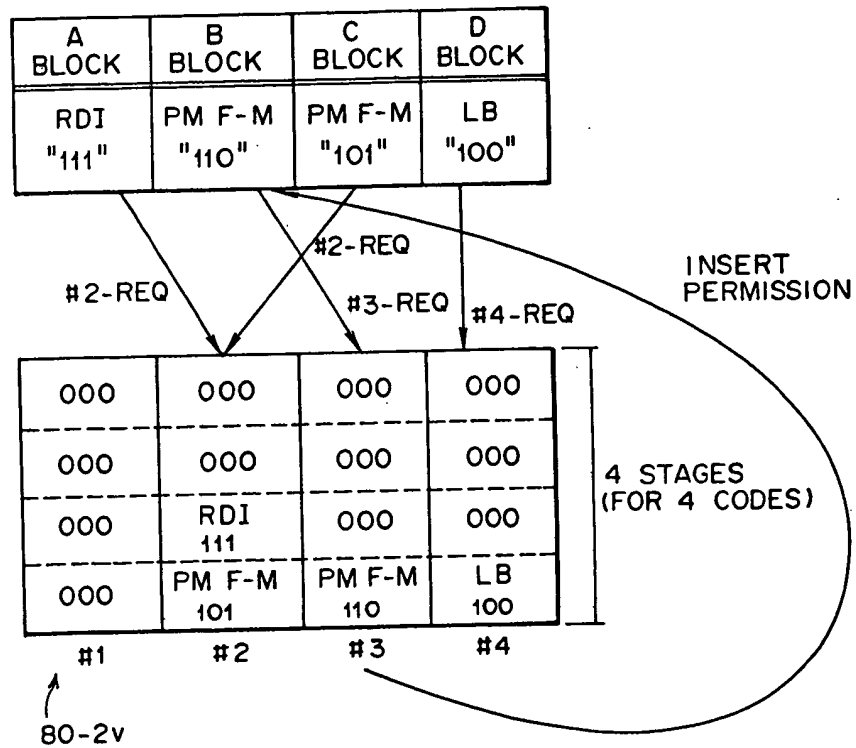


FIG.9



111 A BLOCK: CELL PROCESSING UNIT
 110 B BLOCK: PM PROCESSING UNIT (FM)
 101 C BLOCK: PM PROCESSING UNIT (OTHER THAN FM)
 100 D BLOCK: LB PROCESSING UNIT

FIG. 10(a)

FIG. 10(b)

		[bit]															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
[clk]		GFC				VPI								VCI			
1																	
2																	
3																	
4																	
5																	
6																	
7																	
8																	
9																	
10																	
11																	
12																	
13																	
14																	
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17																	
18																	
19																	
20																	
21																	
22																	
23																	
24																	
25																	
26																	
27																	
28																	

23~28: RDI & LB CELL FORMAT COMMON FIXED PATTERN

Fig. 11

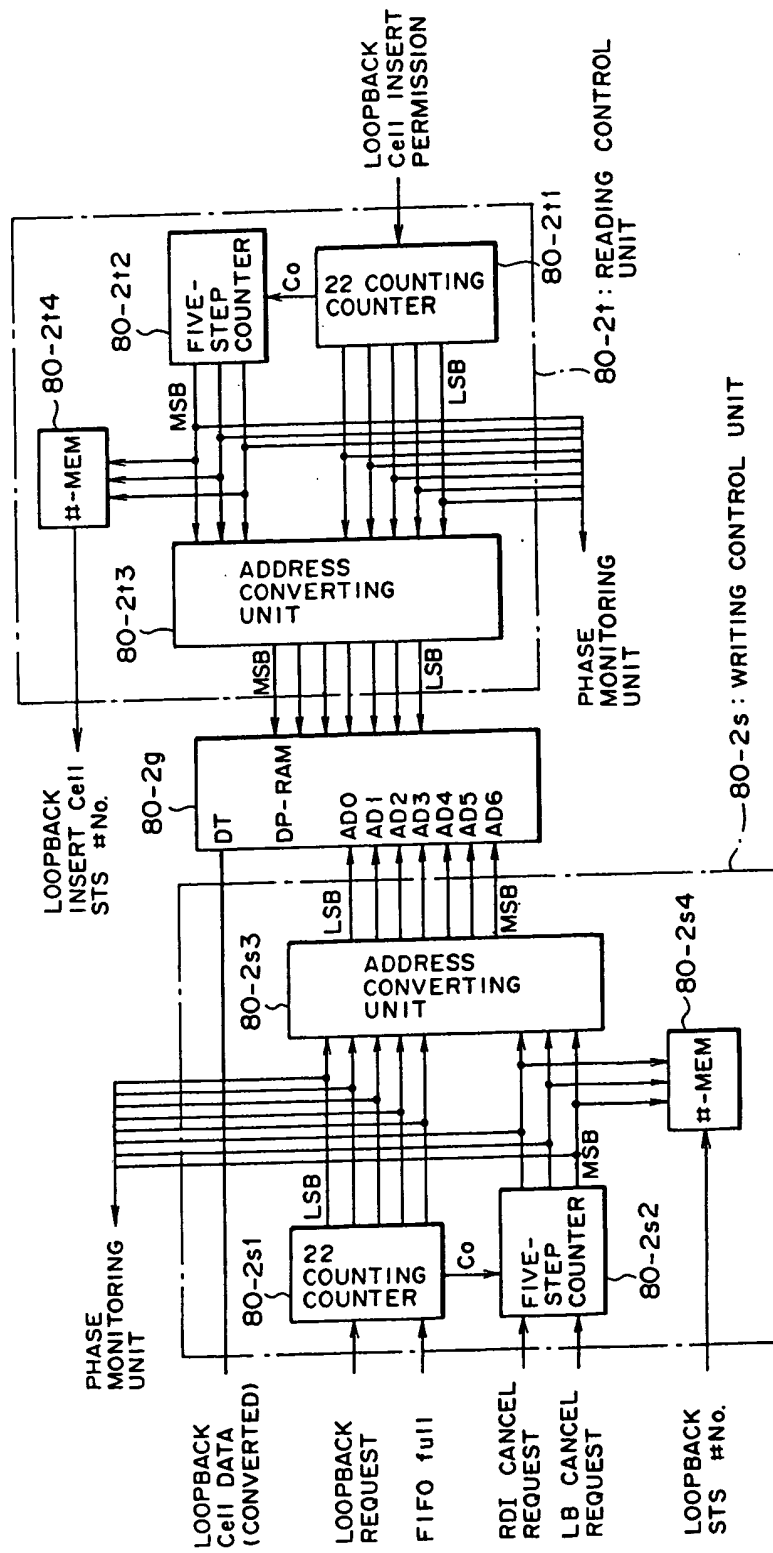


FIG. 12

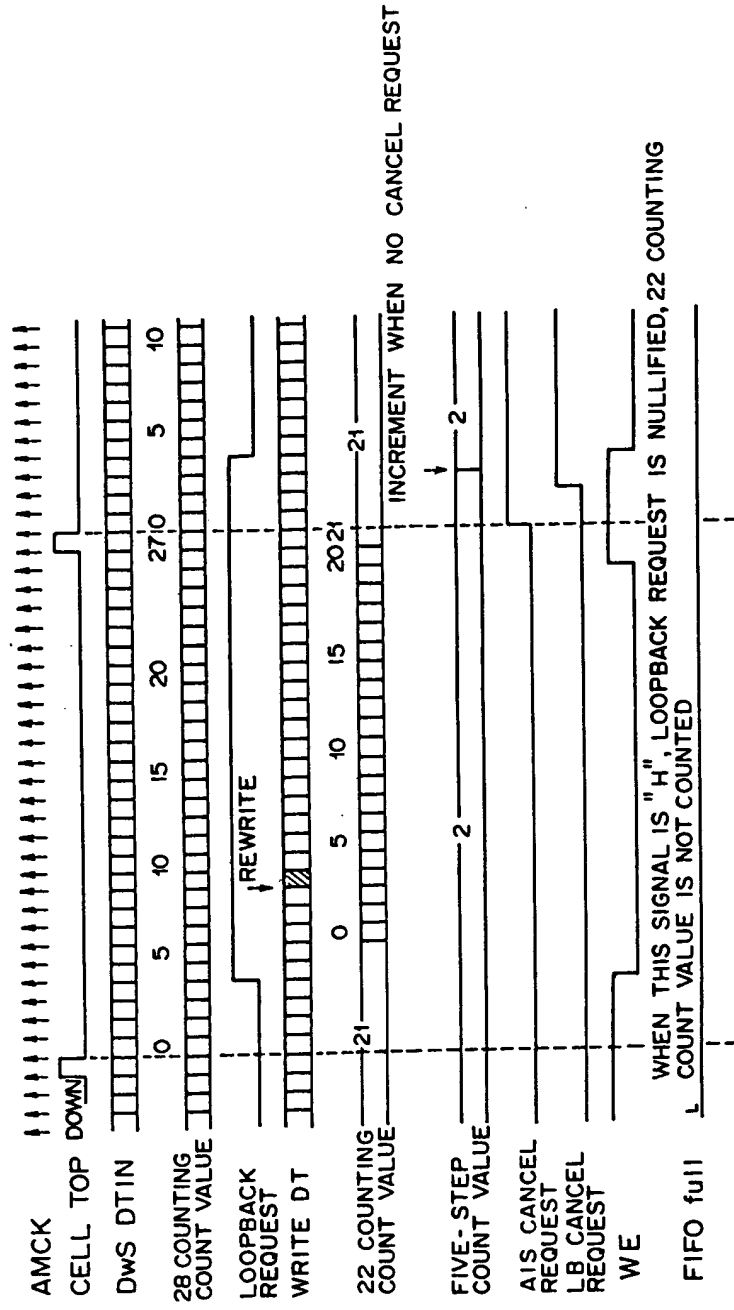


FIG. 13

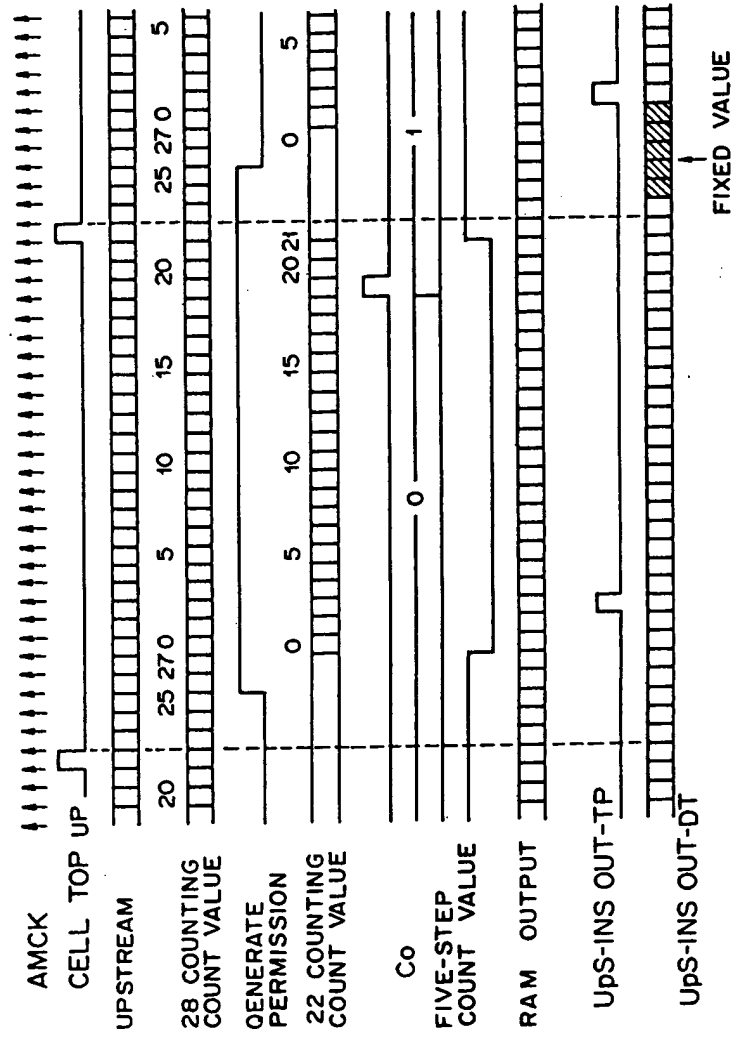


FIG. 14

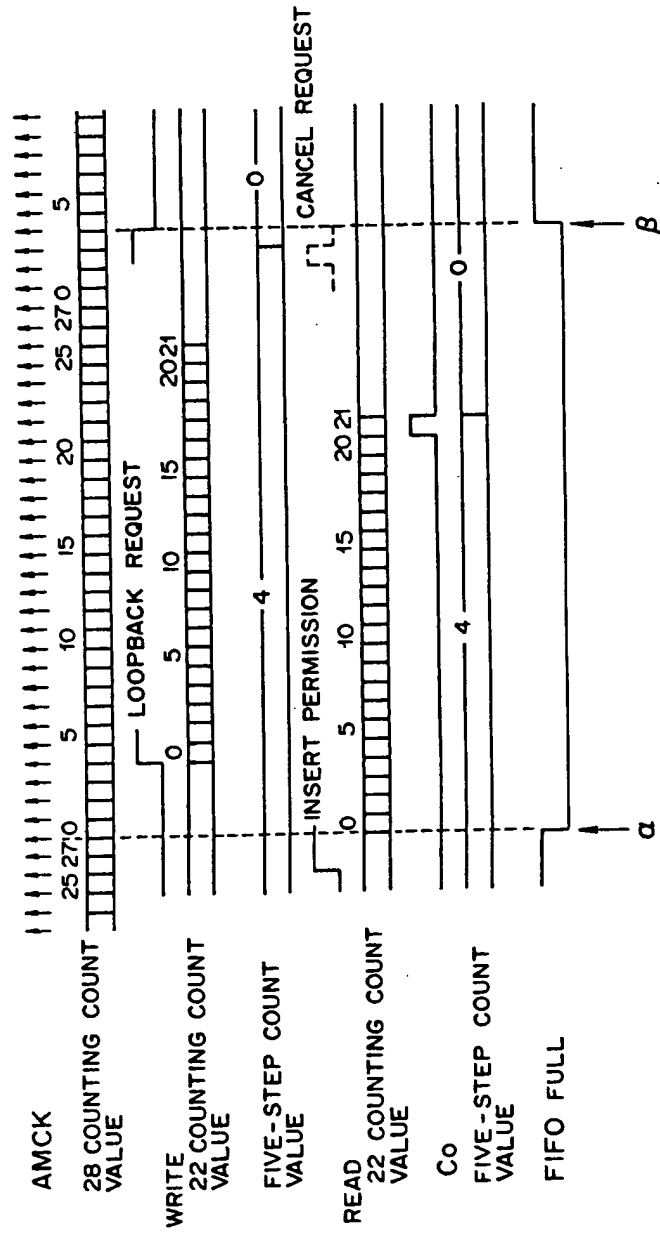


FIG. 15

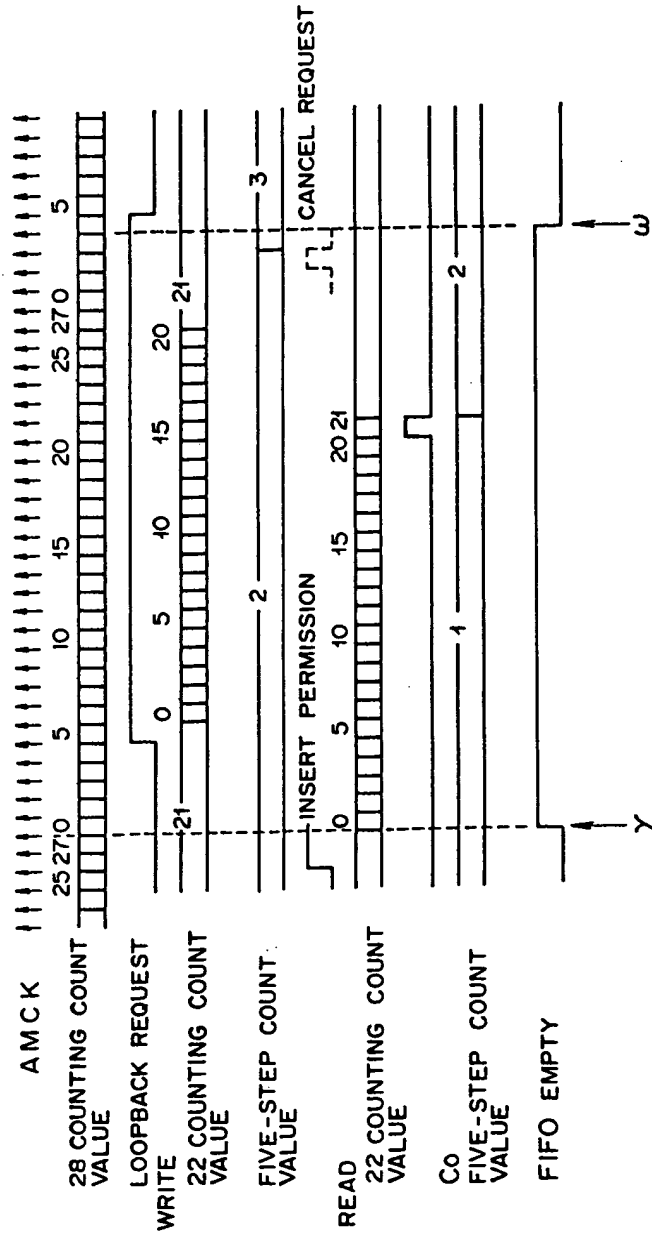


FIG. 16

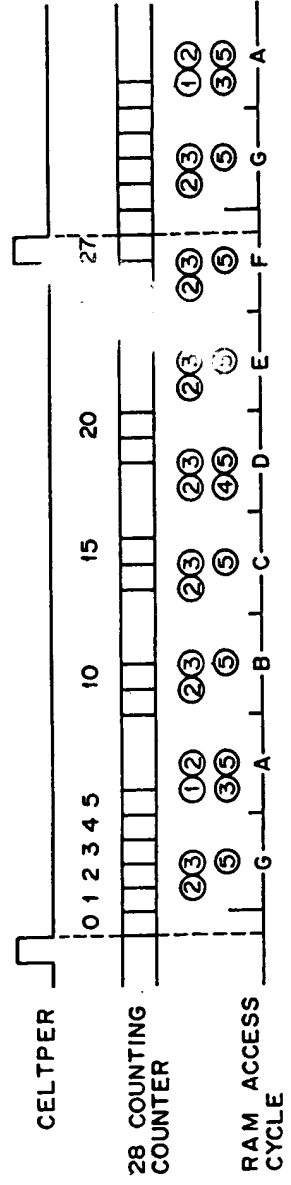


FIG.17

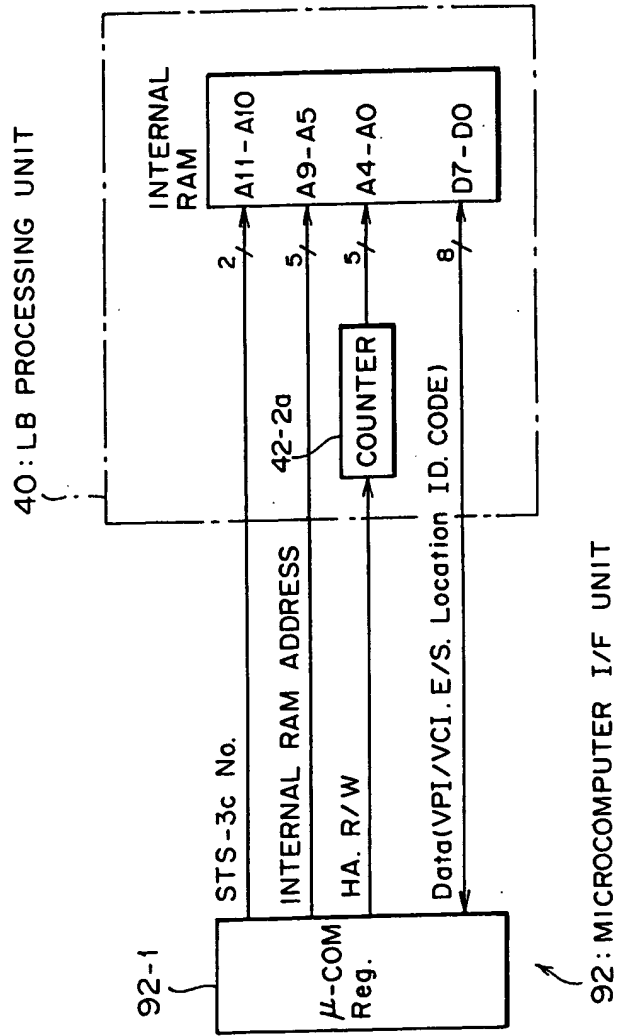
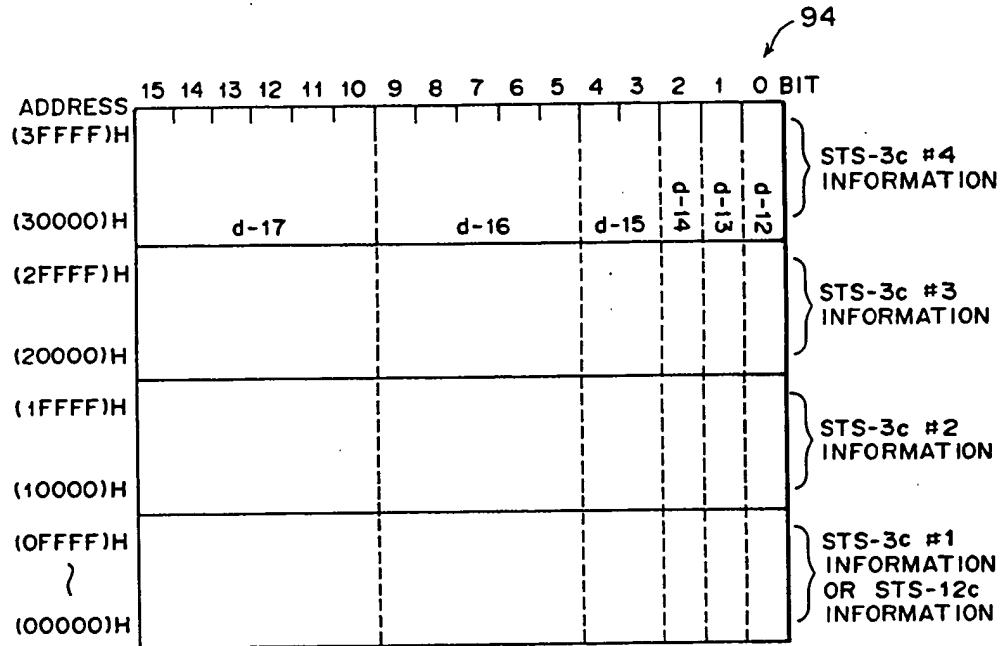


FIG. 18

LSI ADDRESS	D7		D6, D5		D4, D3		D2, D1		D0		REG. STATE
	R/W	STS-3c No.	INTERNAL RAM ADDRESS		VPI/VCI		B8		B0		READ/WRITE
12H	HA										READ/WRITE
13H	B15										READ/WRITE
14H	B7										READ/WRITE
15H											READ/WRITE
16H											READ/WRITE
17H	B127										READ/WRITE
18H	B119										READ/WRITE
19H	B111										READ/WRITE
1AH	B103										READ/WRITE
1BH	B95										READ/WRITE
1CH	B87										READ/WRITE
1DH	B79										READ/WRITE
1EH	B71										READ/WRITE
1FH	B63										READ/WRITE
20H	B55										READ/WRITE
21H	B47										READ/WRITE
22H	B39										READ/WRITE
23H	B31										READ/WRITE
24H	B23										READ/WRITE
25H	B15										READ/WRITE
26H	B7										READ/WRITE
27H											READ ONLY

FIG.19



d-12: ENTRY : WHETHER VPI/VCI IS ENTERED ("H": IN PROCESS OF ENTRY)

d-13: VC TERMINATION : WHETHER VPI/VCI IS TERMINATED. WHEN "H", VPI/VCI IS IN (End-to-End) SETTING.

d-14: OAM INVALID :
WHEN "H", OAM CELL UNDERGOES NO PROCESS, PASSES THROUGH WHEN DETECTED.

d-15: E-to-E / Segment :
DESIGNATE End-to-End / Segment OF VPI/VCI. 2bits EXPRESSES 4 STATES. ONLY TWO STATES OF "01" AND "11" ARE DETERMINED. THE OTHER STATES ARE HANDLED AS INVALID (NO Segment DESIGNATION)

d-16: Loop Back ADDRESS :
SHOW WHICH ch AMONG 32ch THAT ARE OBJECTS OF Loop Back VPI/VCI CORRESPONDS TO

d-17: VC ALM ADDRESS :
SHOW WHICH CHANNEL AMONG 64ch THAT ARE OBJECTS OF VC-AIS/RDI DETECTION VPI/VCI CORRESPONDS TO

FIG. 20

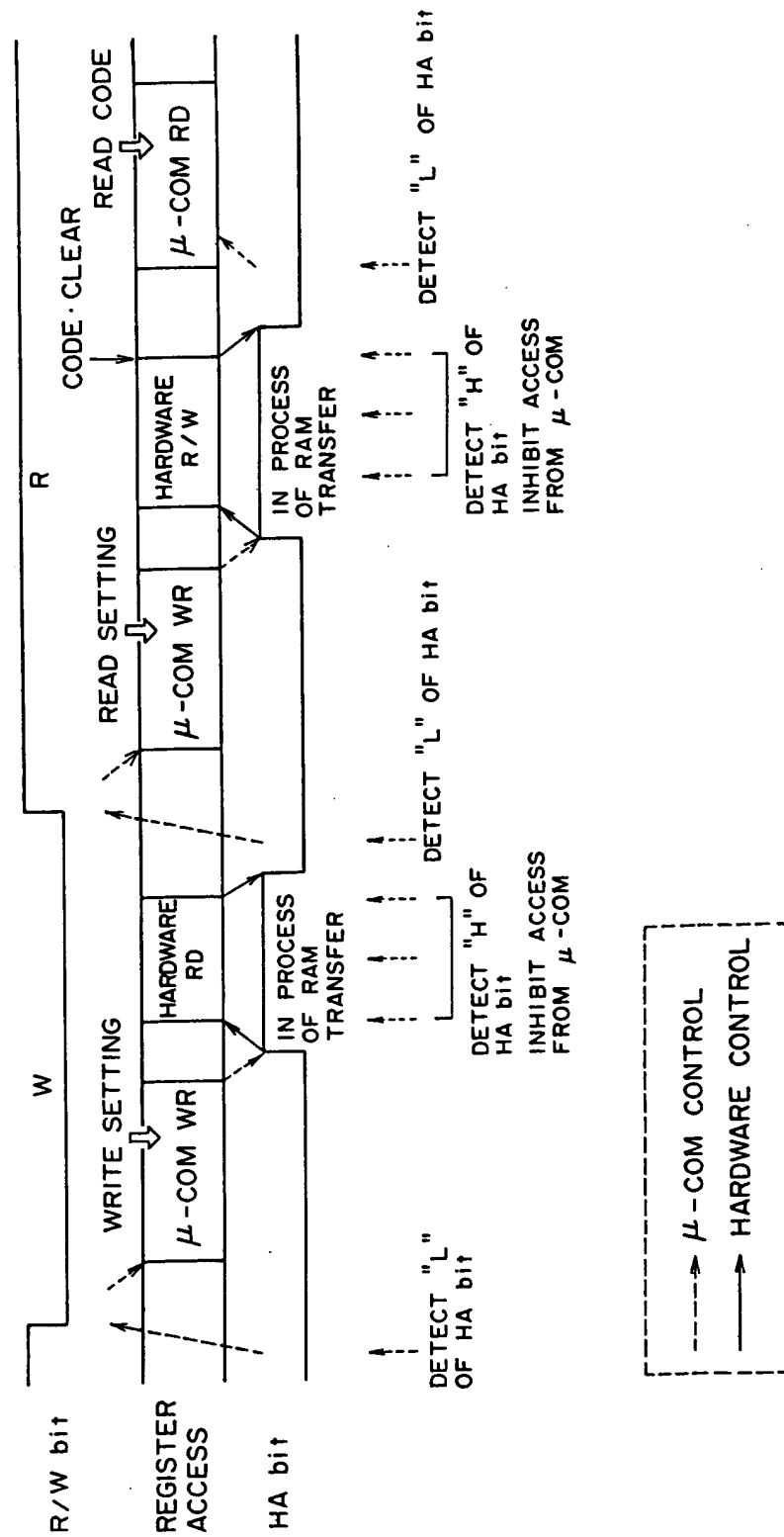


FIG. 21

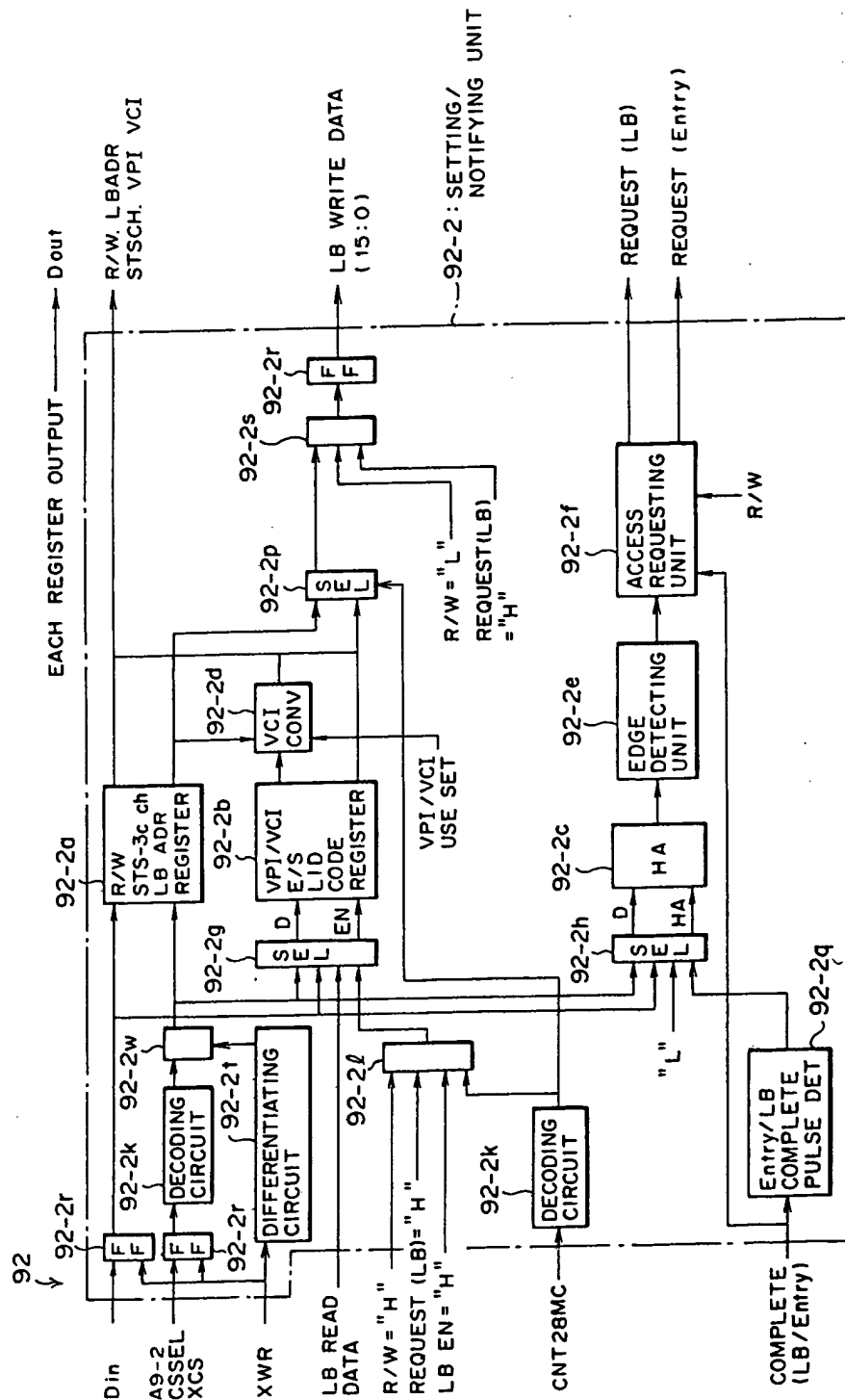


FIG. 22

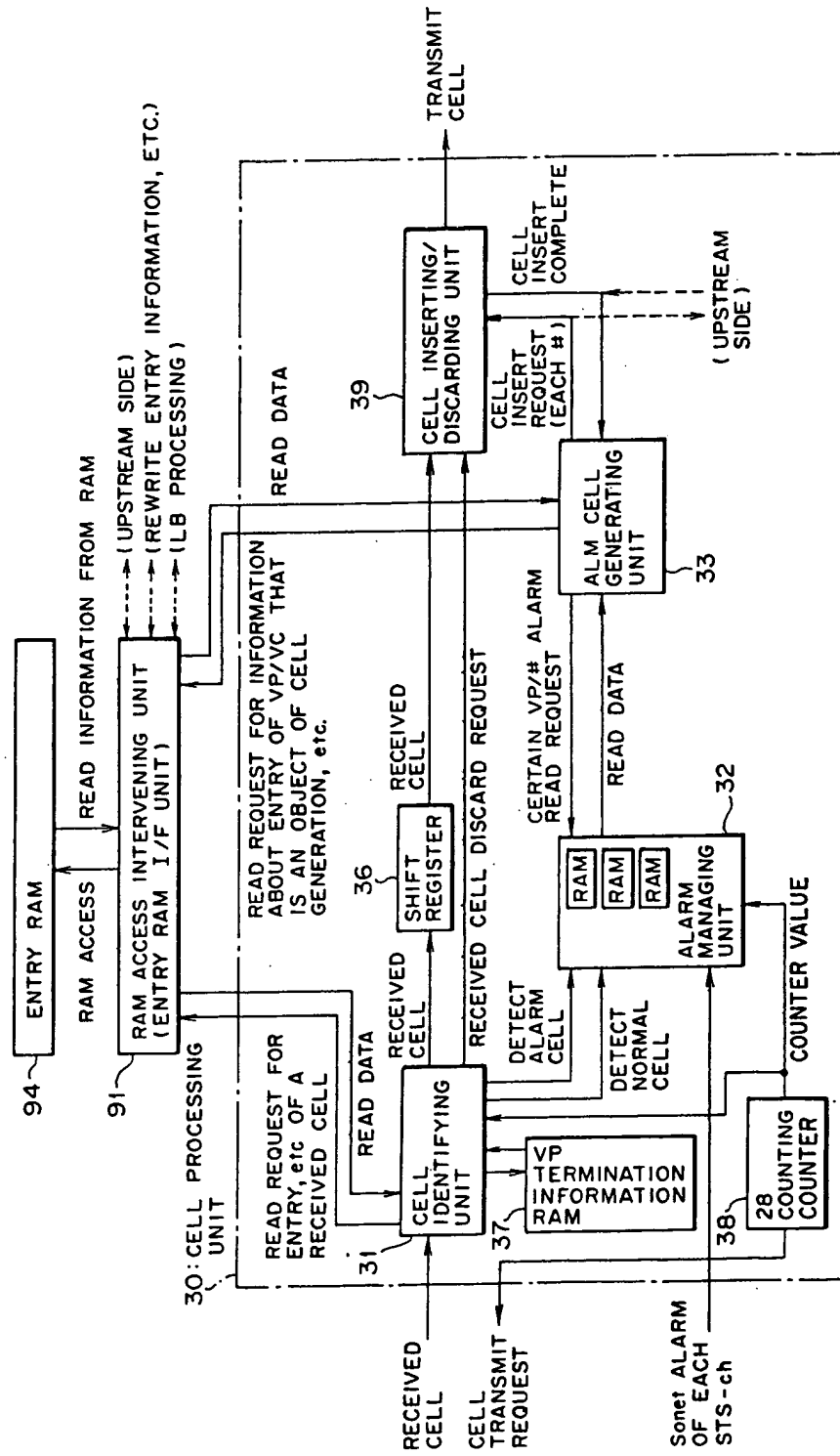
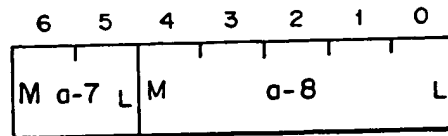
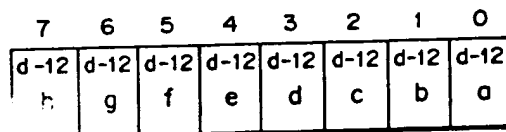


FIG. 23



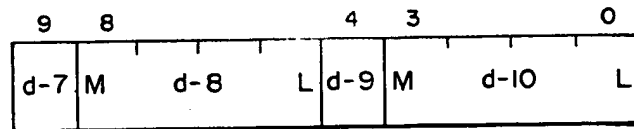
a-7: SHOW STS - 3c # 00: STS-3c #1 or STS-12C
 01: STS-3c #2
 10: STS-3c #3
 11: STS-3c #4
 a-8: VPI (HIGH ORDER 5 bits AMONG 8bits)

FIG. 24



"H": VP
 "L": NORMAL

FIG.25



- d-7 : SHOW VC-AIS STATE ("H": AIS)
- d-8 : CANCELING TIMER FOR VC-AIS
2.5 SECOND COUNTER, COUNTED UP
EVERY 156msec
- d-9 : SHOW VC-RDI STATE ("H": RDI)
- d-10: CANCELING TIMER FOR VC-RDI,
2.5 SECOND COUNTER,
COUNTED UP EVERY 156msec

FIG. 26

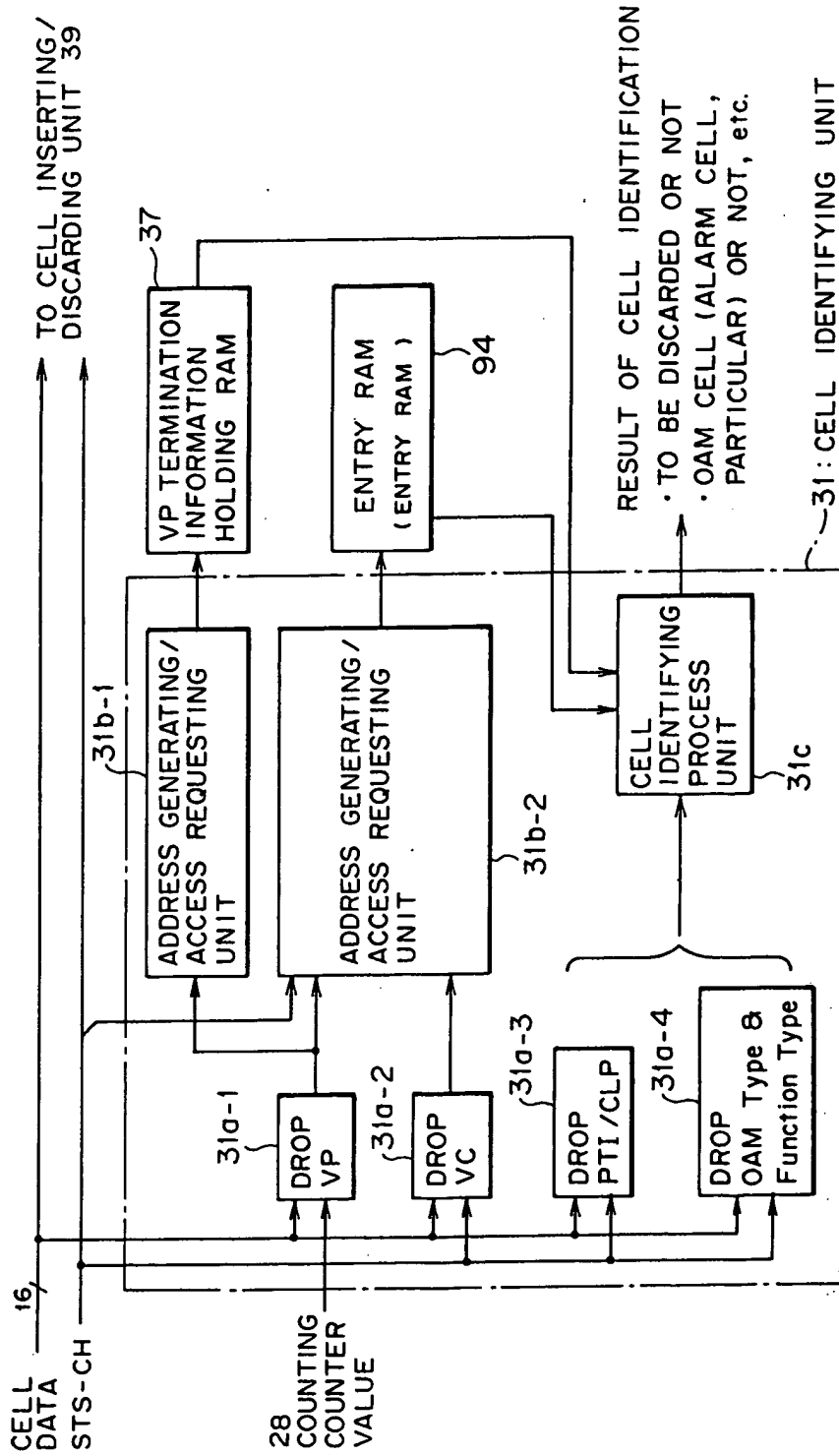


FIG. 27

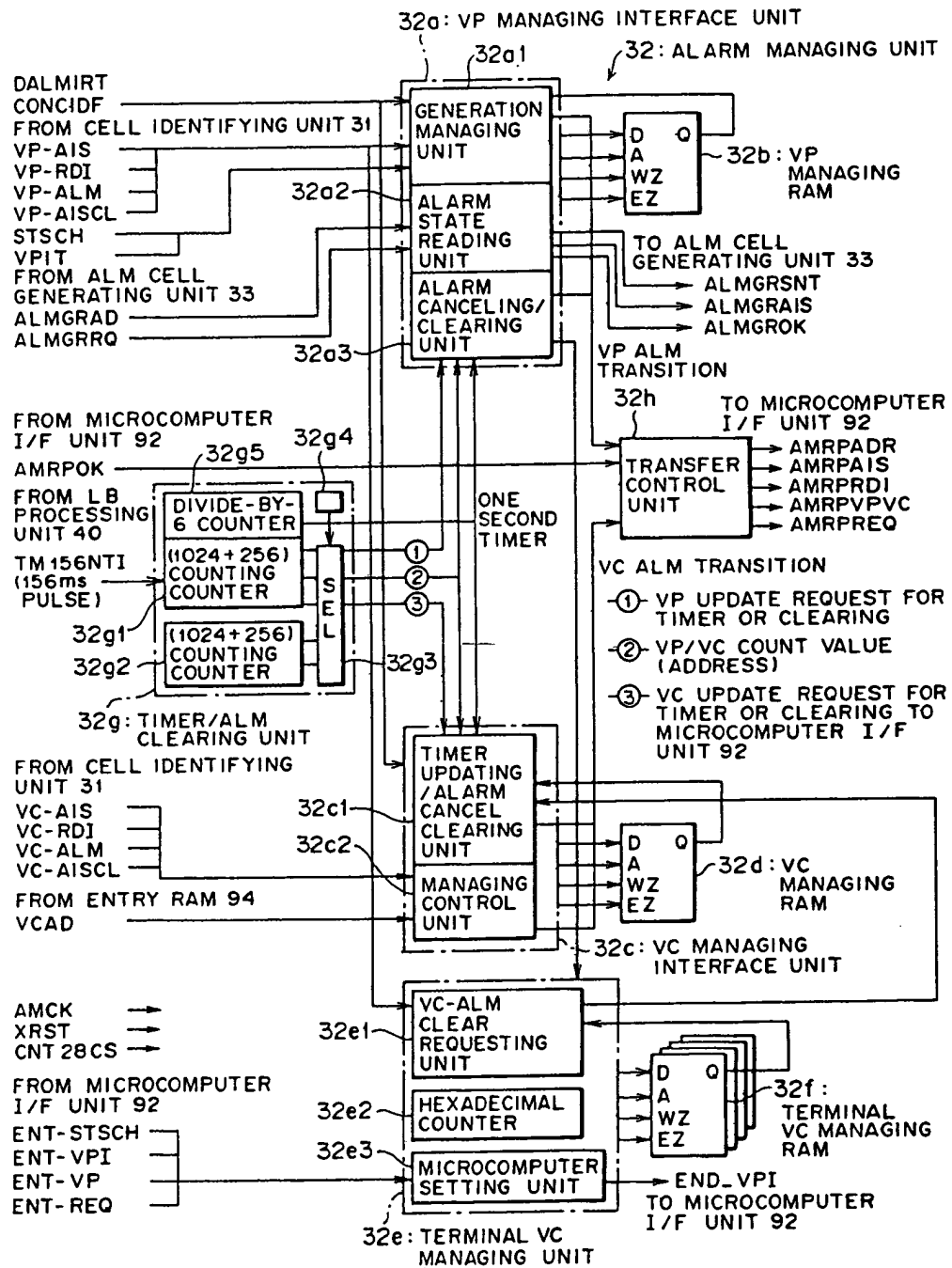
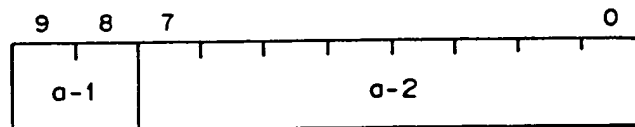


FIG.28



a-1 : STS-3c IDENTIFICATION ADDRESS

00: STS-3c #1 / STS-12c

01: STS-3c #2

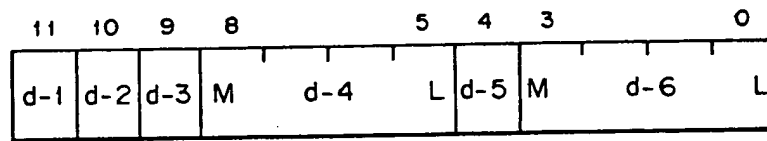
10: STS-3c #3

11: STS-3c #4

a-2 : VPI (8 bits) OF ALM Cell

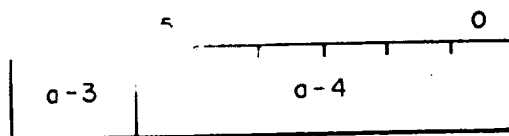
WHEN VPI IS LESS THAN 8bits,
ADD "0" TO HIGH ORDER bits

FIG.29



- d-1 : SHOW VP-AIS STATE ("H":AIS)
- d-2 : FLAG "500mF" SHOWING WHETHER ALARM CELL IS
SENT WITHIN THE INITIAL 500msec AFTER GETTING
INTO VP -AIS STATE OR SONET ALM STATE
("L":SEND COMPLETE)
("H":SEND NOT COMPLETE)
- d-3 : FLAG "1sF" USED TO SEND ALARM CELL AT 1 sec
INTERVALS
- d-4 : VP-AIS CANCELING TIMER,
2.5 SECOND COUNTER, COUNTED UP EVERY 156 msec
- d-5 : SHOW VP-RDI STATE ("H":RDI)
- d-6 : VP-RDI CANCELING TIMER,
2.5 SECOND COUNTER, COUNTED UP EVERY 156 msec

FIG.30



a-3 : STS-3c IDENTIFICATION ADDRESS

00: STS-3c #1 / STS-12c

01: STS-3c #2

10: STS-3c #3

11: STS-3c #4

a-4 : VC-AIS/RDI MANAGING INTERNAL ADDRESS
(VC-ALM ADDRESS SET IN ENTRY RAM)
(0~63)

FIG. 31

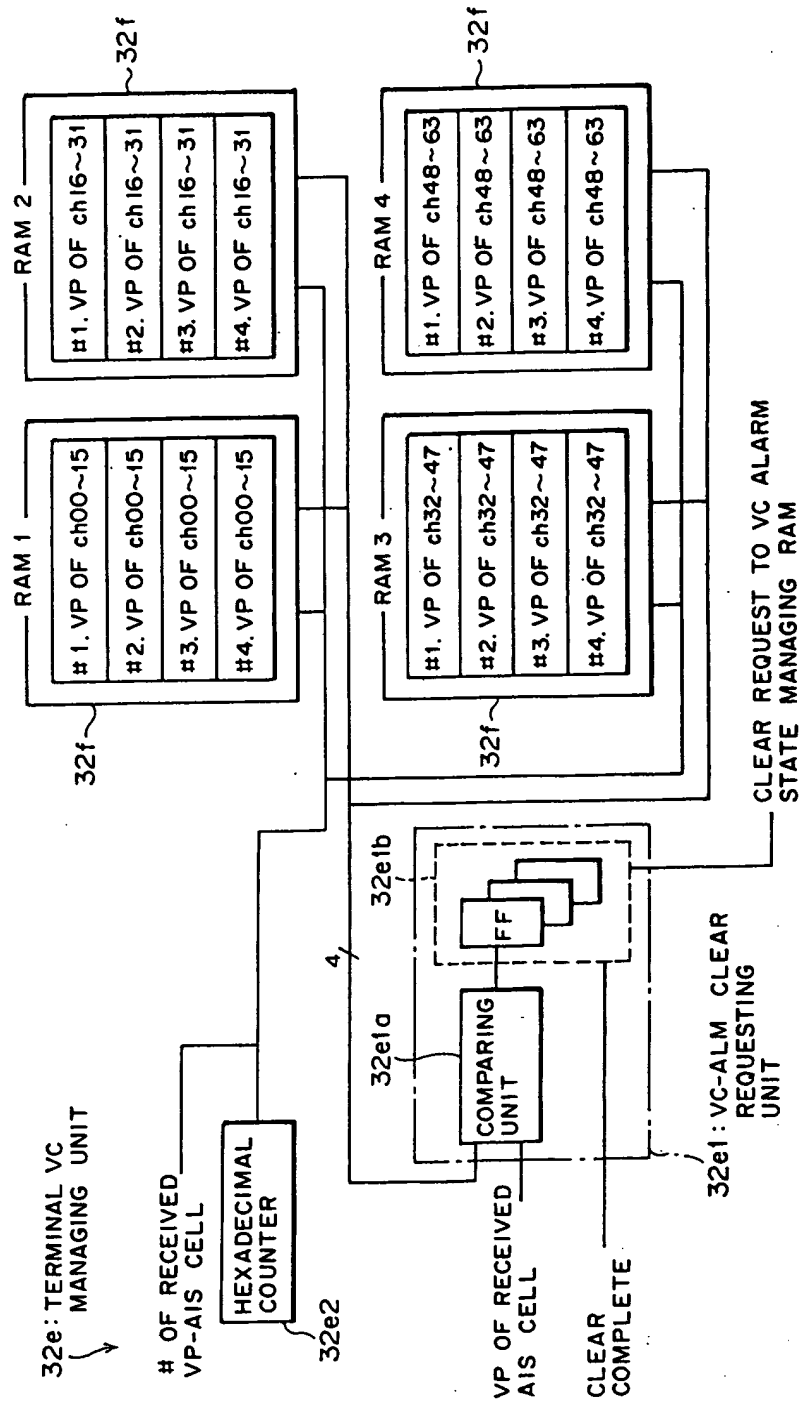
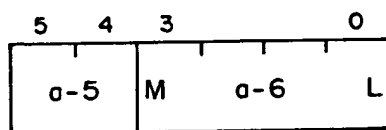


FIG.32



a-5 : STS-3c IDENTIFICATION ADDRESS

00: STS-3c #1 / STS-12c

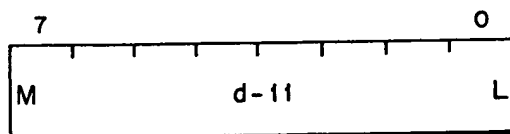
01: STS-3c #2

10: STS-3c #3

11: STS-3c #4

a-6 : LOW ORDER 4bits OF VC TERMINATION
SETTING ch(6bits)

FIG.33



d-11 : HOLD VPI OF VPI/VC1 TO WHICH VC
TERMINATION IS SET

FIG.34

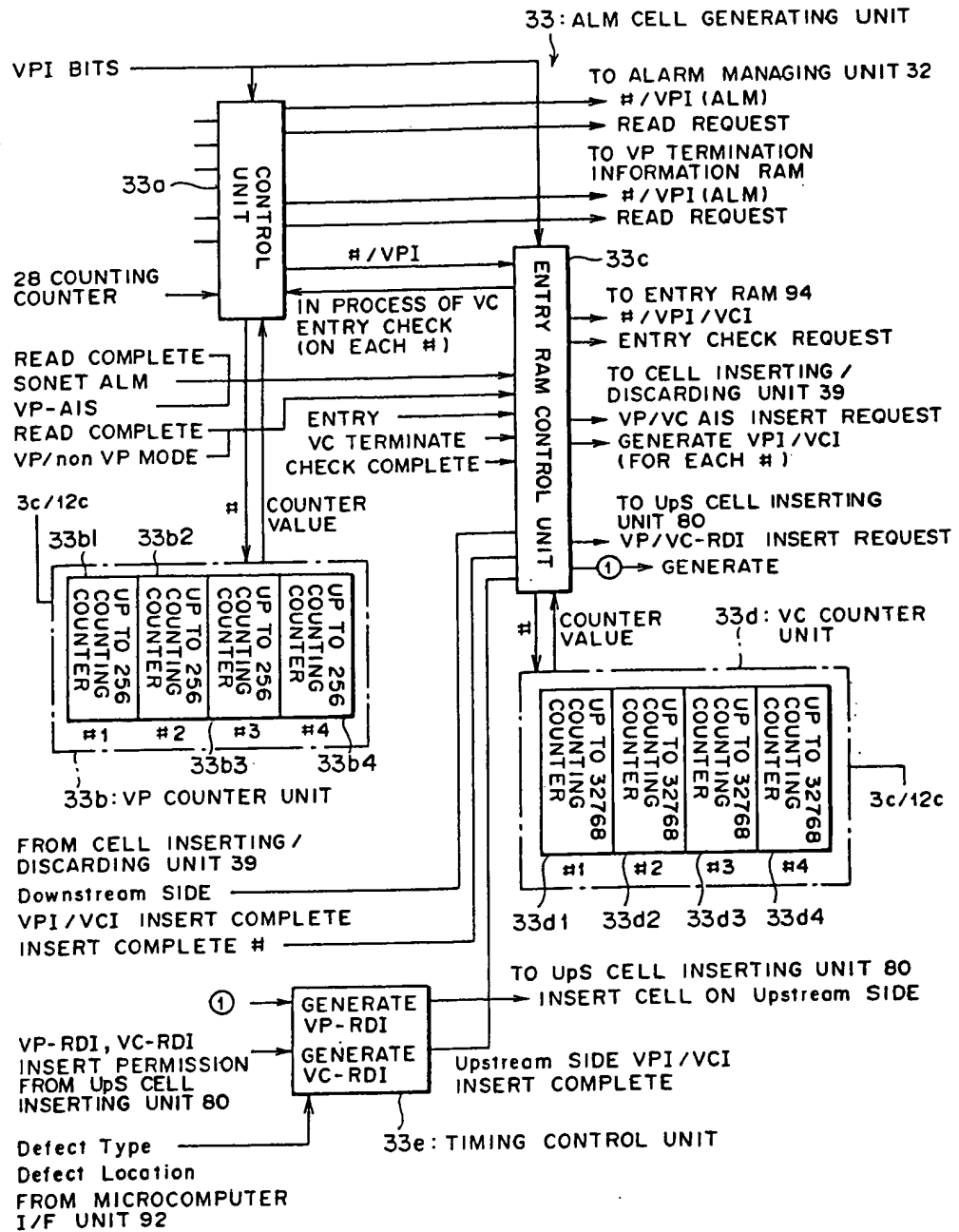


FIG.35

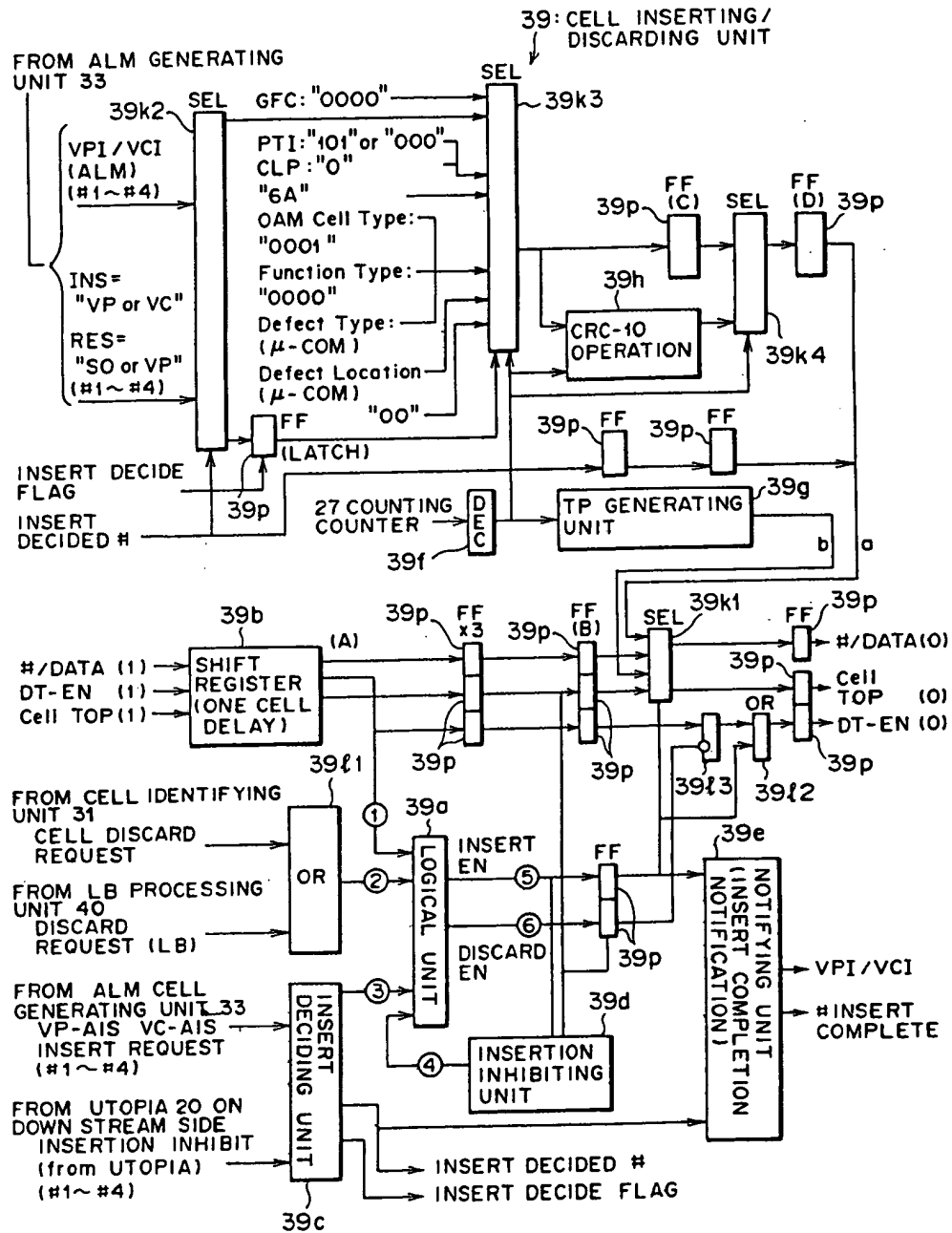


FIG.36

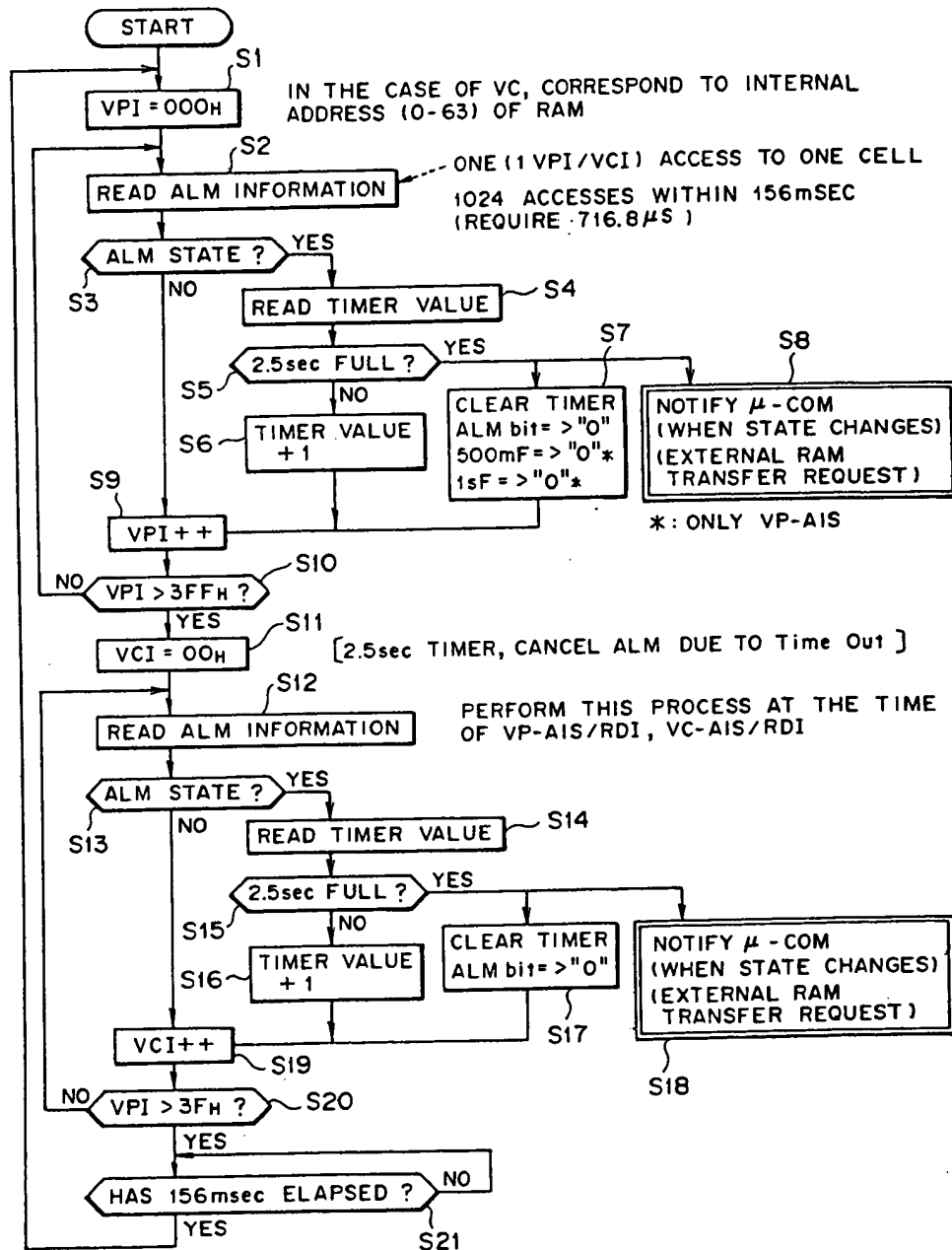


FIG. 37

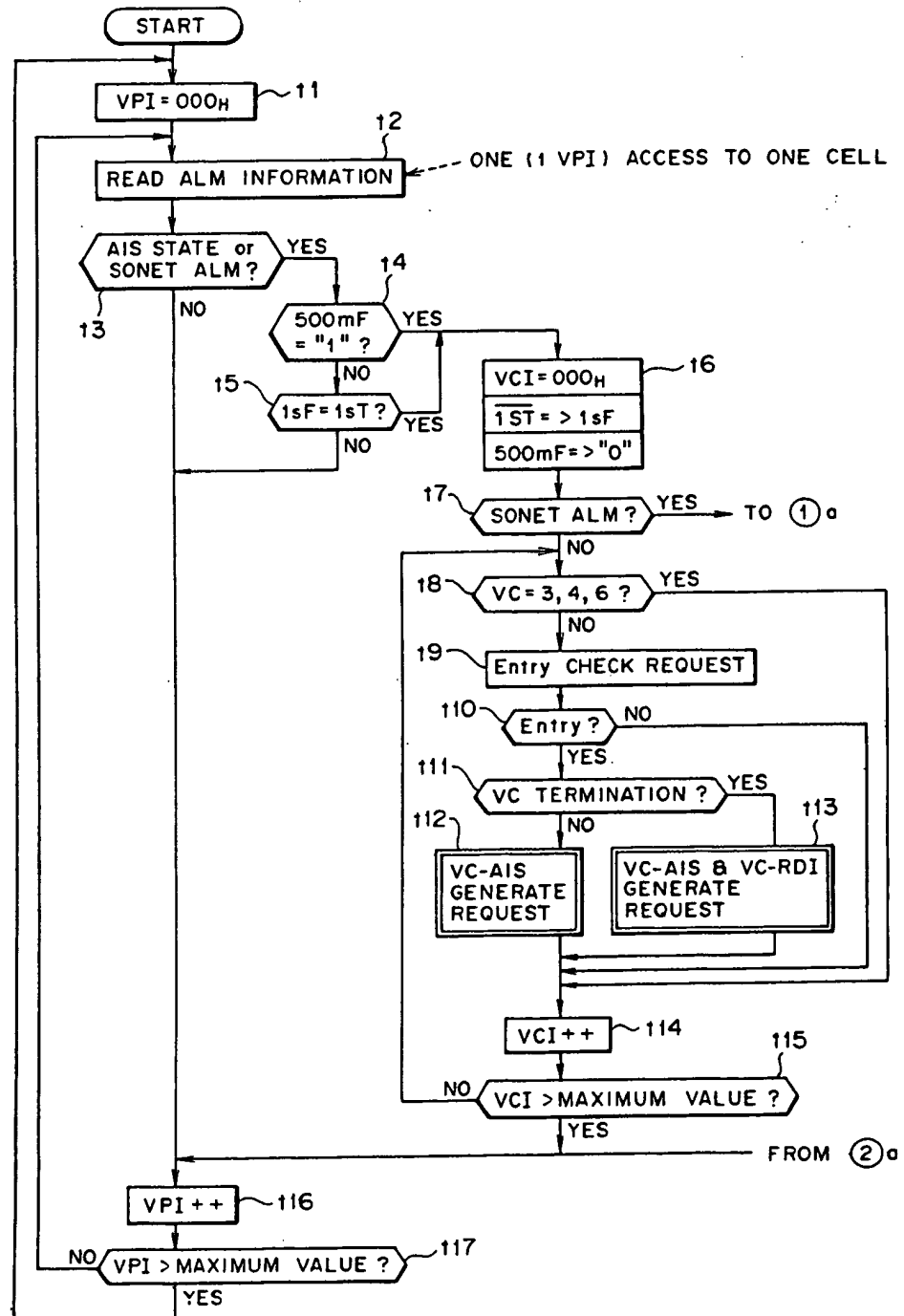
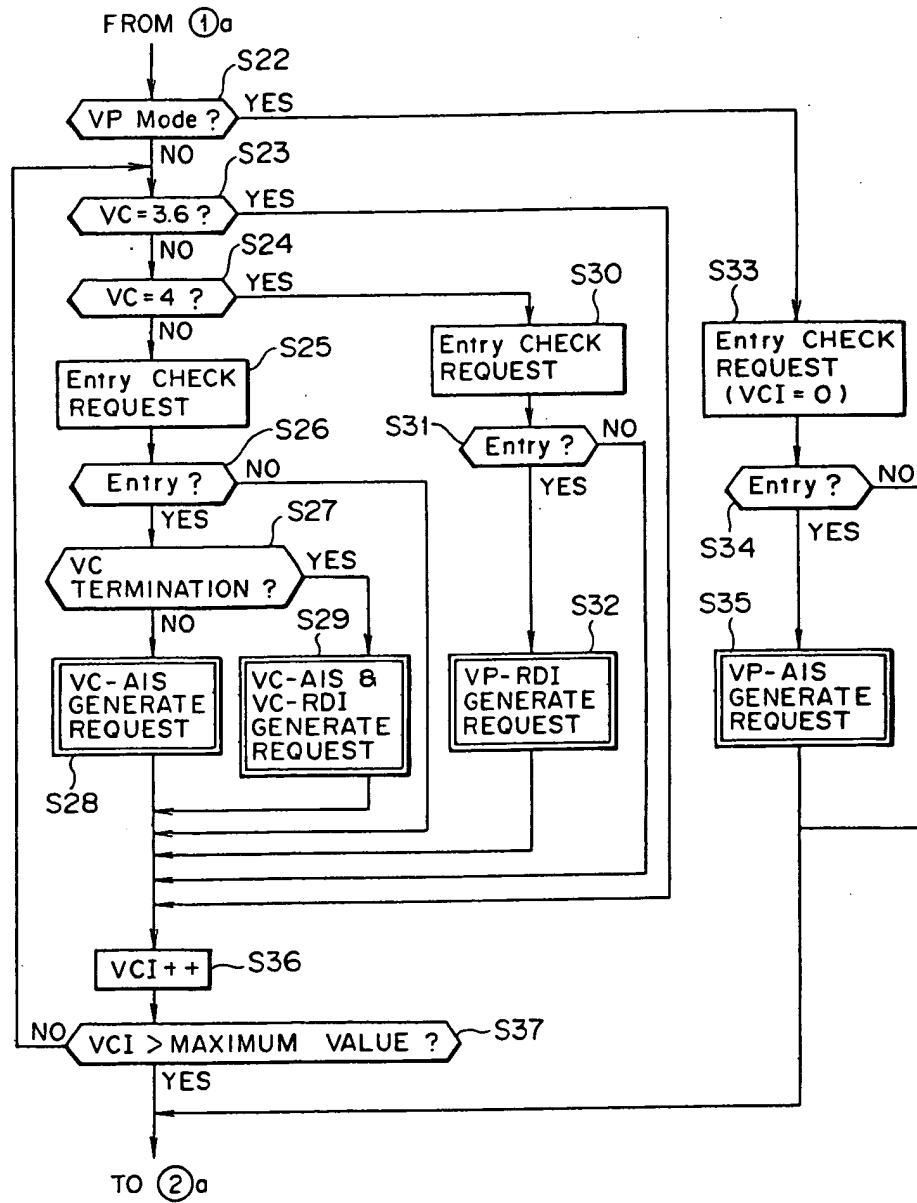


FIG.38



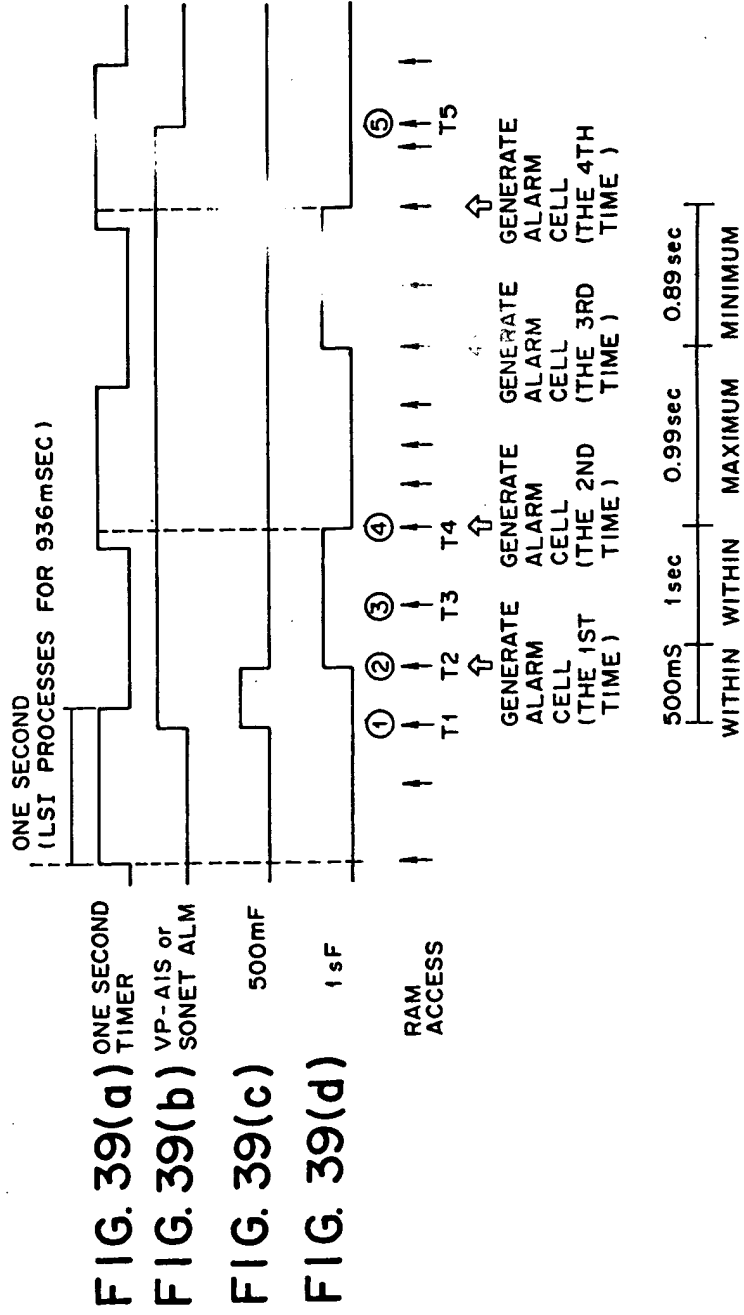


FIG.40

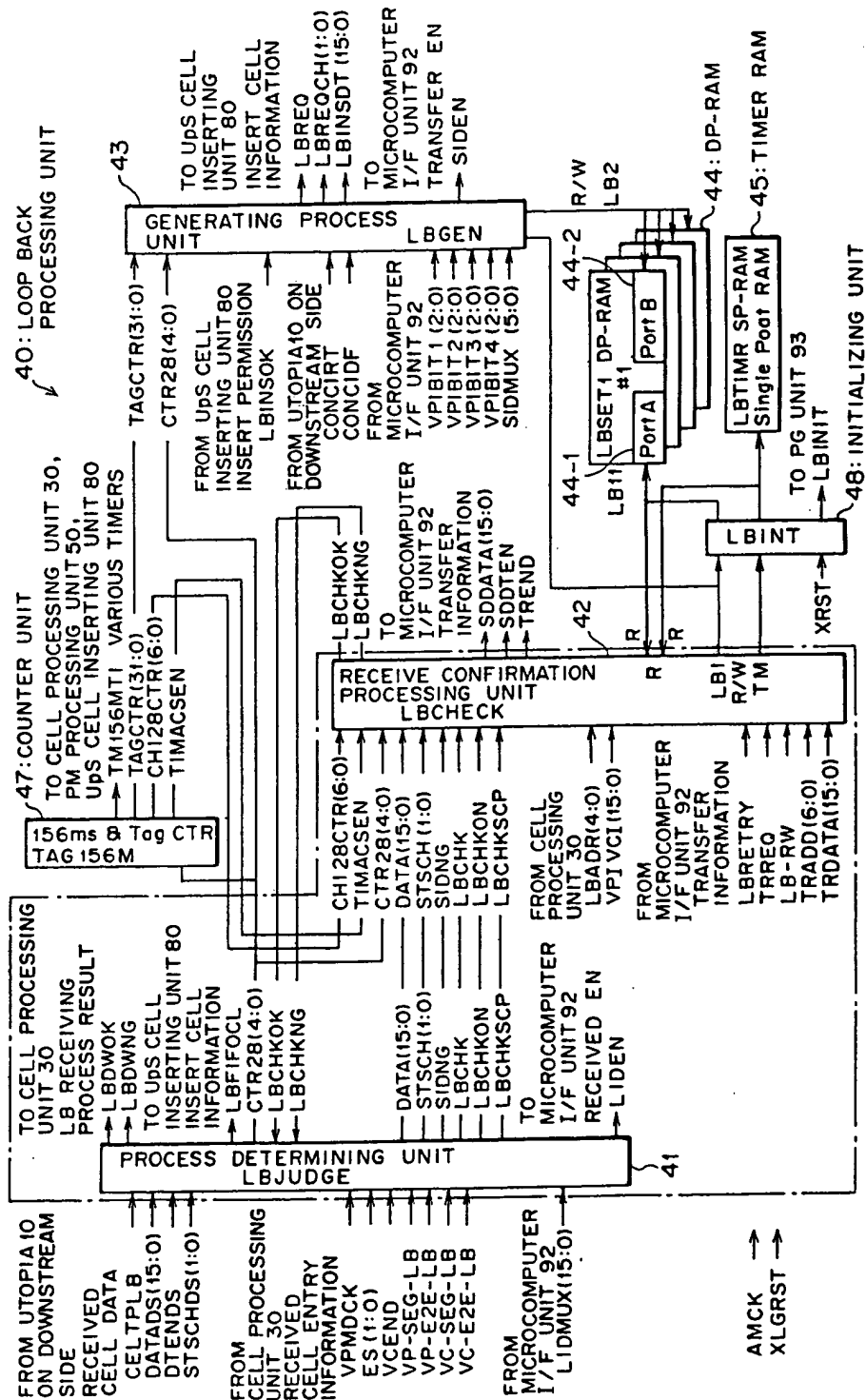


FIG.41

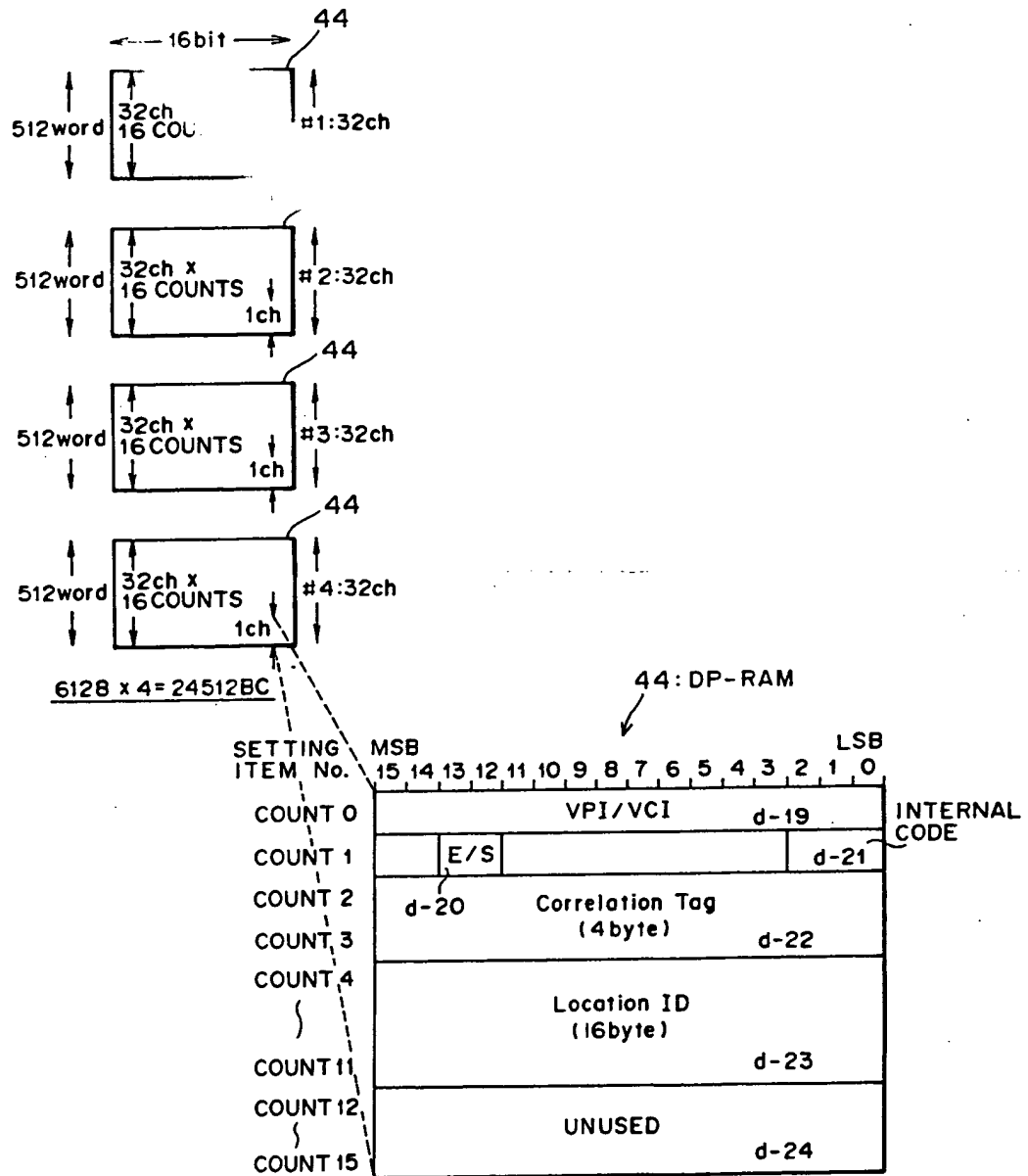


FIG.42

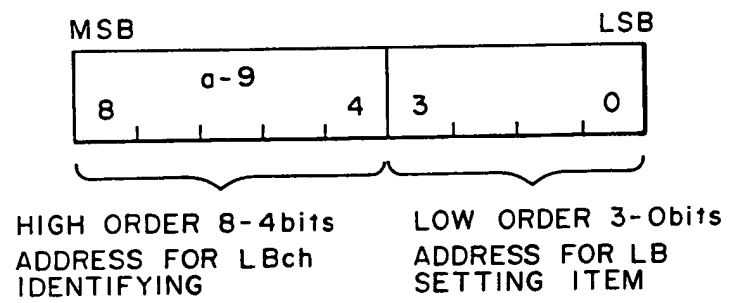
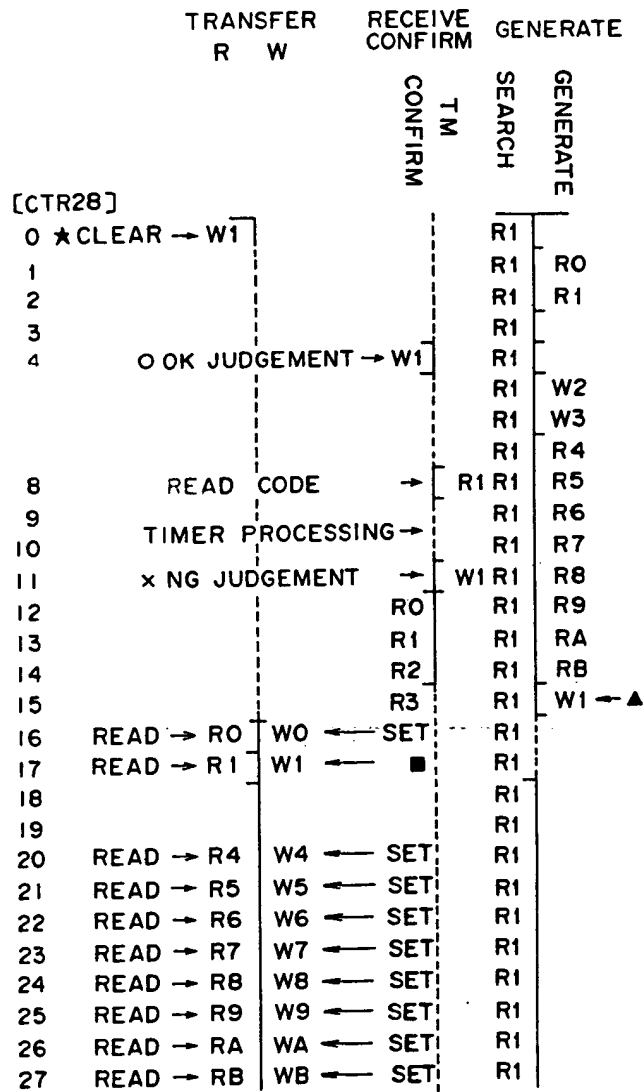


FIG.43



- ★ : CLEAR code AFTER OK/NG CODE IS READ
- O : WRITE OK code RESULTING FROM OK JUDGEMENT
- x : WRITE NG code RESULTING FROM TIME OUT
- : WRITE transmit wait code AT THE TIME OF MICROCOMPUTER SETTING AND CLEAR TIMER
- ▲ : WRITE receive wait code WHEN LB CELL IS GENERATED

FIG. 44

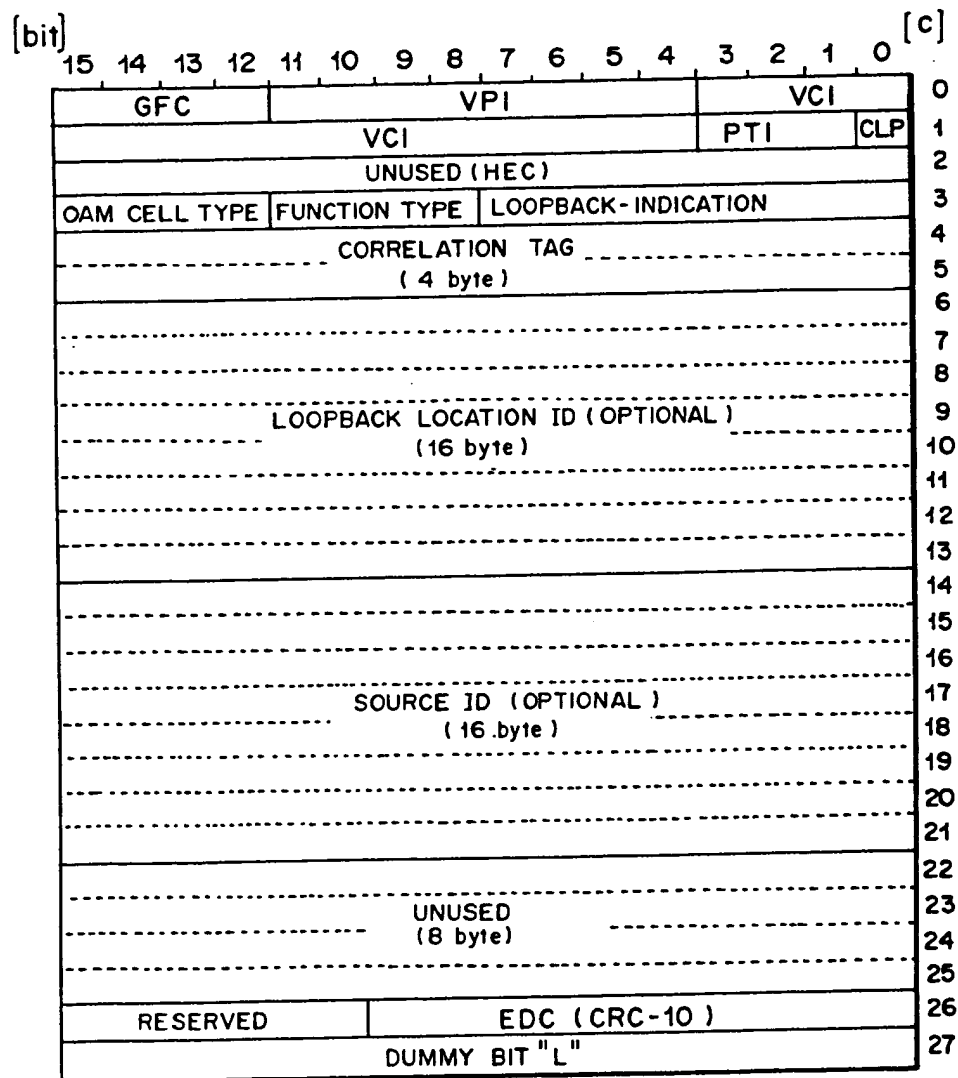


FIG. 45

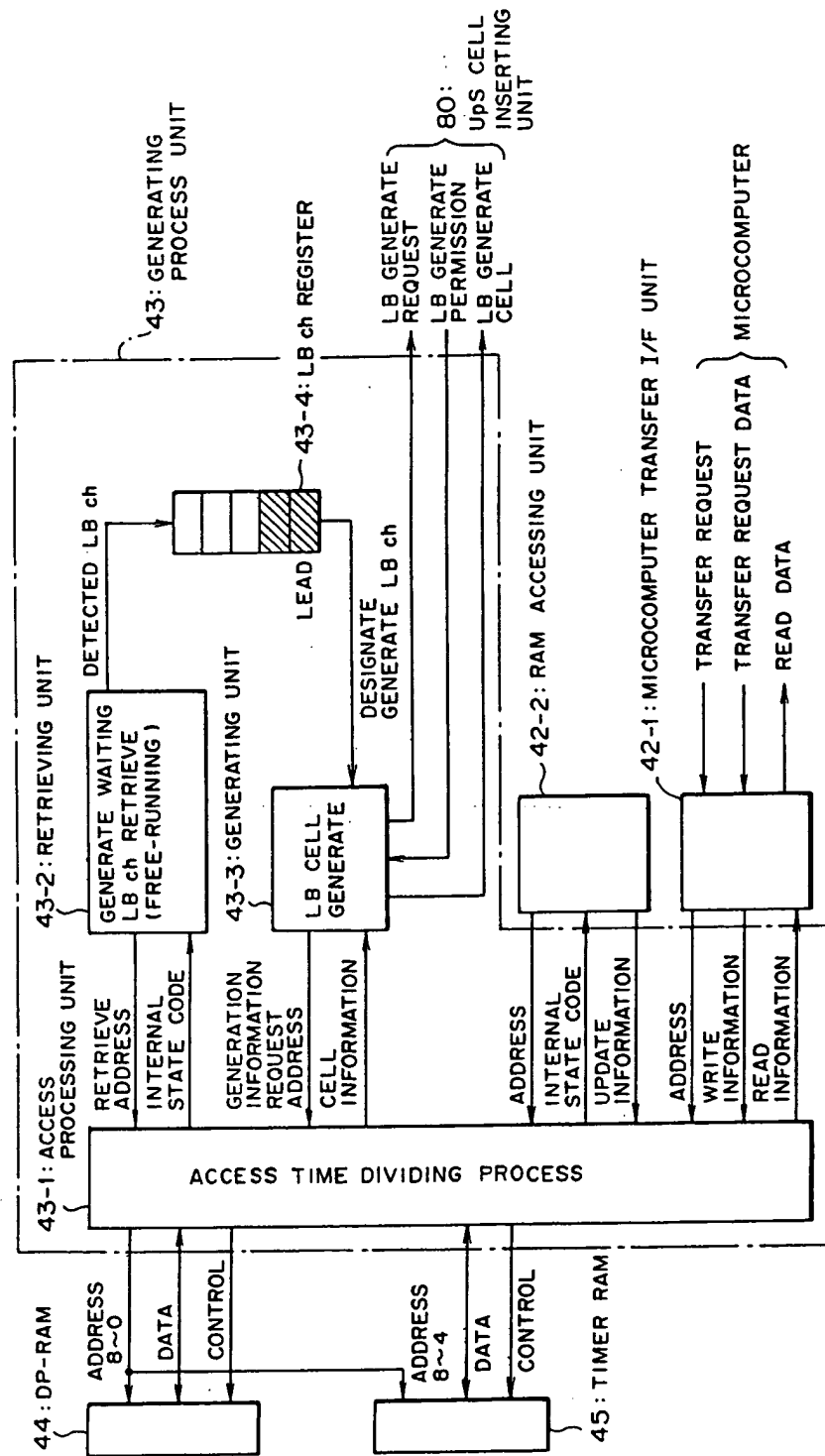


FIG. 46

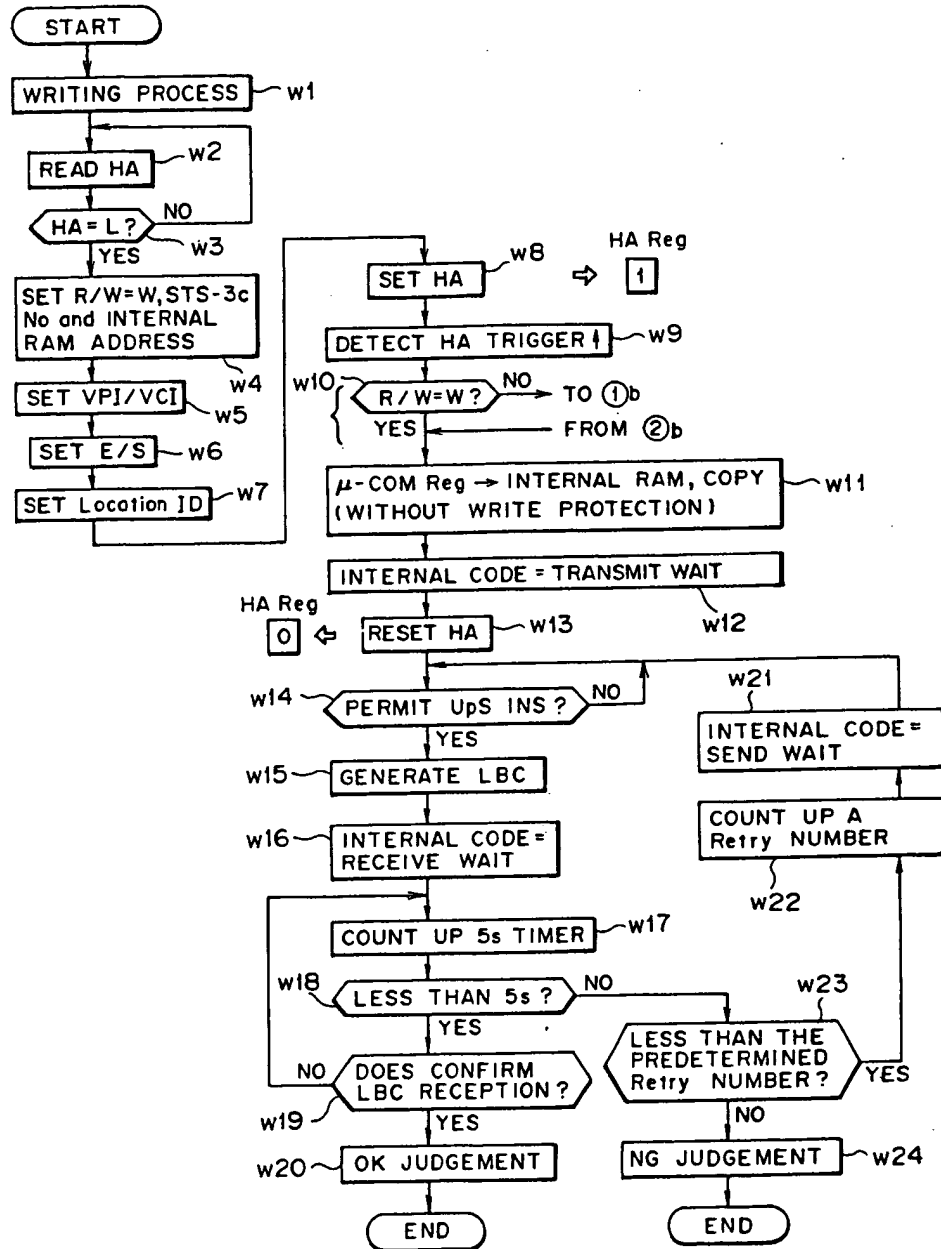


FIG.47

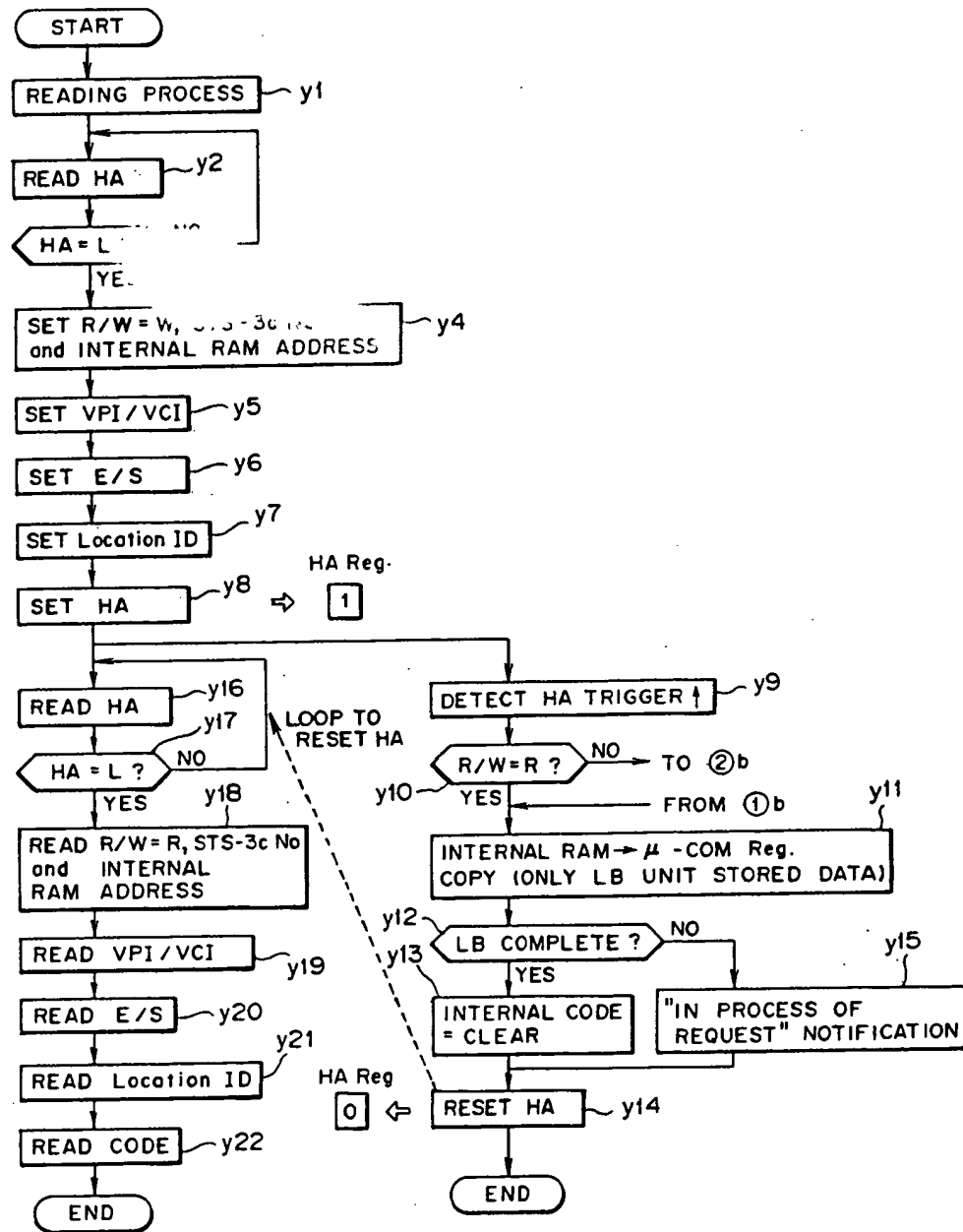


FIG. 48

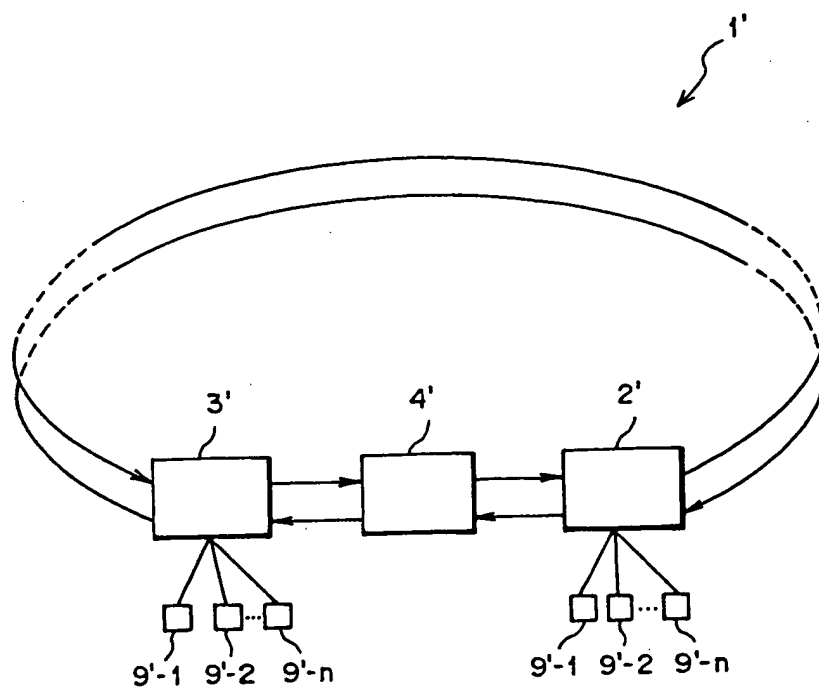


FIG. 49

